

# **54/74 Families of Compatible TTL Circuits**

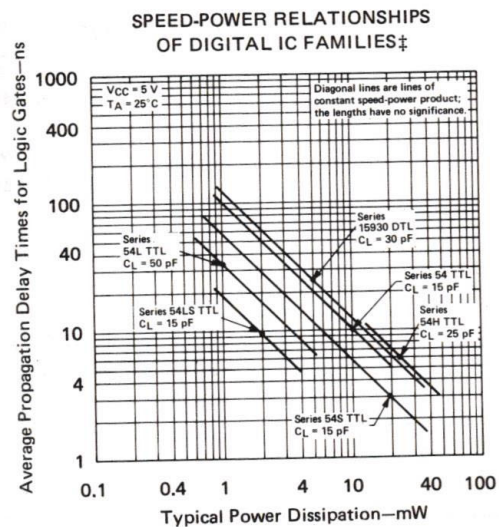
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

OCTOBER 1976

## description

Texas Instruments transistor-transistor-logic (TTL) family of high-performance bipolar digital integrated circuits comprises five distinct series of compatible product lines. These product lines offer the digital systems designer a full spectrum of performance ranges in order to optimize system cost and performance. The available choices range from the very high performance of the Schottky-clamped<sup>†</sup> functions for systems operating typically up to 125 megahertz to low-power functions with power consumption of only one milliwatt per gate.

Typical characteristics of the five TTL series offered are shown in Table I and their respective speed/power relationships are illustrated in Figure A.



† Typical saturated logic gate from the indicated families.

FIGURE A

TABLE I—54/74 FAMILY TYPICAL SSI PERFORMANCE CHARACTERISTICS

SERIES	GATES			FLIP-FLOPS
	Speed-Power Product	Propagation Delay Time	Power Dissipation	Clock Input Frequency Range
54LS/74LS	19 pJ	9.5 ns	2 mW	dc to 45 MHz
54L/74L	33 pJ	33 ns	1 mW	dc to 3 MHz
54S/74S	57 pJ	3 ns	19 mW	dc to 125 MHz
54/74	100 pJ	10 ns	10 mW	dc to 35 MHz
54H/74H	132 pJ	6 ns	22 mW	dc to 50 MHz

## features

### EASE OF SYSTEM DESIGN

- Full compatibility provides choice from five distinct performance ranges
- Broad range of functions are offered in each series
- Diode-clamped inputs are provided on all high-performance functions
- Terminated, controlled-impedance lines are not normally required with TTL
- Low output impedance:
  - Provides low a-c noise susceptibility
  - Drives high-capacity loads

### FULL COMPATIBILITY IS DESIGNED INTO TI TTL

- All series are designed for single 5-volt power supply
- All series provide one-volt or greater typical d-c noise margins
- Power dissipation relatively insensitive to operating frequency
- Switching times are guaranteed at full d-c loading
- Compatible with most logic families such as DTL, MOS, CMOS

<sup>†</sup> Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	54 FAMILY	SERIES 54 SERIES 54H	SERIES 54L	SERIES 54LS	SERIES 54LS	SERIES 54S	UNIT
	74 FAMILY	SERIES 74 SERIES 74H	SERIES 74L	SERIES 74LS WITH DIODE INPUTS	SERIES 74LS WITH EMITTER INPUTS	SERIES 74S	
Supply voltage, $V_{CC}$ (see Note 1)		7	8	7	7	7	V
Input voltage		5.5	5.5	7	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5		5.5	5.5	V
Off-state (high-level) voltage applied to open-collector outputs of SSI circuits (see Note 3)	'06, '07	30					V
	'16, '17, '26	15					
	Others		8	7	7	7	
High-level voltage applied to a disabled 3-state output		5.5		5.5	5.5	5.5	V
Operating free-air temperature range	54 Family	-55 to 125					°C
	74 Family	0 to 70					
Storage temperature range		-65 to 150					°C

- NOTES: 1. Voltage values, unless otherwise noted, are with respect to network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies between inputs that go directly into the same  $\overline{\text{AND}}$  or NAND gate in the functional block diagram.  
 3. Ratings for MSI parts are given on the individual data sheets.

5

### unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than  $V_{OH \text{ min}}$  (see tables of electrical characteristics), but not to exceed the absolute maximum rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling unused inputs are:

- Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between  $V_{OH \text{ min}}$  and 4.5 V. Series 54LS/74LS devices with diode inputs may be connected directly to  $V_{CC}$ .
- Connect unused inputs to a used input if maximum drive capability of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
- Connect unused inputs to  $V_{CC}$  through a 1-k $\Omega$  resistor so that if a transient that exceeds the input maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-k $\Omega$  resistor. Series 54LS/74LS devices with diode inputs may be connected directly to  $V_{CC}$ .
- Connect unused inputs to any fixed-high-level compatible output such as the output of an inverter or NAND gate that has its input(s) grounded. Maximum high-level drive capability of the output should not be exceeded.

## 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

### input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and  $V_{CC}$  ranges. The table below shows maximum input current requirements and nominal base resistor values for standard loads in each TTL series. A standard load is defined as an input connected to a single emitter or diode that is associated with a pull-up resistor having the value indicated in the table. However, some inputs are tied to more than one input transistor (or diode), or the base-resistor values of some inputs have been changed either to reduce input-current requirements or to improve performance. Therefore, the input-current requirements may vary. Consult the electrical characteristics table for the particular device type to determine the input-current requirements of each input.

STANDARD INPUTS (ONE LOAD)

SERIES	NOMINAL VALUE OF INPUT PULL-UP RESISTOR	MAXIMUM HIGH-LEVEL INPUT CURRENT	MAXIMUM LOW-LEVEL INPUT CURRENT
54/74	4 k $\Omega$	40 $\mu$ A	-1.6 mA
54H/74H	2.8 k $\Omega$	50 $\mu$ A	-2 mA
54L/74L ‡	40 k $\Omega$	10 $\mu$ A	-0.18 mA
	8 k $\Omega$	20 $\mu$ A	-0.8 mA
54LS/74LS	18 k $\Omega$	20 $\mu$ A	-0.4 mA
54S/74S	2.8 k $\Omega$	50 $\mu$ A	-2 mA

‡Series 54L/74L has two different types of standard inputs as shown.

Since low-level input current is primarily a function of the input base resistor, two or more inputs of the same NAND or AND gate may be tied together and still be considered one load at a low logic level, but at a high logic level, each input is an additional load.

Currents into input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

### drive capability

The maximum value of  $I_{OL}$  given under "recommended operating conditions" reflects the ability of an output to sink current from a number of loads at a low voltage level and maximum  $I_{OH}$  reflects the ability to supply current at a high voltage level. Each standard output at a low level is capable of sinking current from 10 standard loads of its own series (20 standard loads for Series 74L and 74LS), and at a high level is capable of supplying current to either 10 or 20 loads of its own series. The fan-out of 20 at a high logic level makes it possible to tie as many as 10 unused inputs of NAND or AND gates to used inputs of the same gates (as mentioned under input-current requirements) without exceeding the fan-out capability of the output driving 10 used inputs. Certain outputs are designed for special applications and have greater or lesser drive capability. See the recommended operating conditions for each type.

The loads may be intermixed in any desired combination so long as the load totals for  $I_{IH}$  and  $I_{IL}$  are less than the maximum recommended values of  $I_{OH}$  and  $I_{OL}$ , respectively, for the driving circuit.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

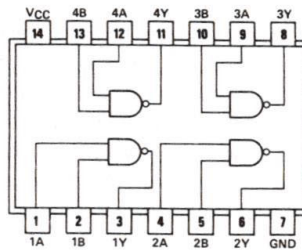
## PIN ASSIGNMENTS (TOP VIEWS)

### QUADRUPLE 2-INPUT POSITIVE-NAND GATES

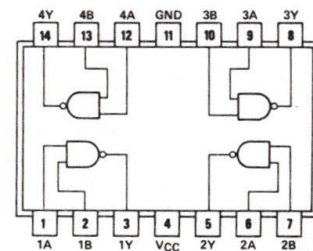
**00**

positive logic:  
 $Y = \overline{AB}$

See page 6-2



SN5400 (J)      SN7400 (J, N)  
 SN54H00 (J)    SN74H00 (J, N)  
 SN54L00 (J)    SN74L00 (J, N)  
 SN54LS00 (J, W) SN74LS00 (J, N)  
 SN54S00 (J, W) SN74S00 (J, N)

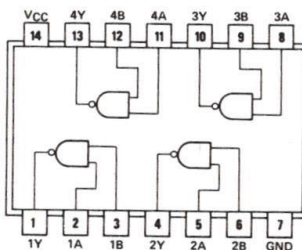


SN5400 (W)  
 SN54H00 (W)  
 SN54L00 (T)

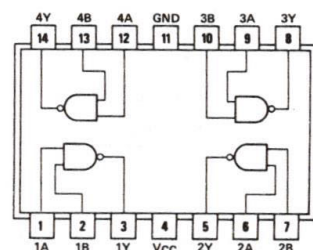
### QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

**01**

positive logic:  
 $Y = \overline{AB}$

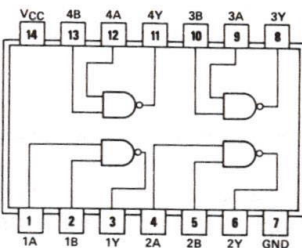


SN5401 (J)      SN7401 (J, N)  
 SN54LS01 (J, W) SN74LS01 (J, N)



SN5401 (W)  
 SN54H01 (W)  
 SN54L01 (T)

See page 6-4



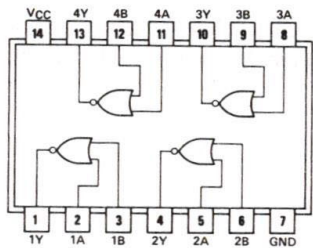
SN54H01 (J)    SN74H01 (J, N)

### QUADRUPLE 2-INPUT POSITIVE-NOR GATES

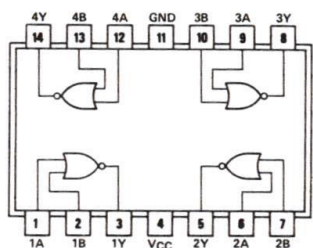
**02**

positive logic:  
 $Y = \overline{A+B}$

See page 6-8



SN5402 (J)      SN7402 (J, N)  
 SN54L02 (J)    SN74L02 (J, N)  
 SN54LS02 (J, W) SN74LS02 (J, N)  
 SN54S02 (J, W) SN74S02 (J, N)



SN5402 (W)  
 SN54L02 (T)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

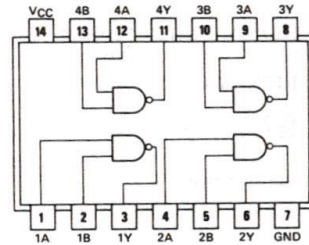
## PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT  
POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS

**03**

positive logic:  
 $Y = \overline{AB}$

See page 6-4



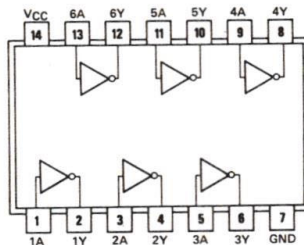
SN5403 (J)      SN7403 (J, N)  
SN54L03 (J)    SN74L03 (J, N)  
SN54LS03 (J, W) SN74LS03 (J, N)  
SN54S03 (J, W) SN74S03 (J, N)

HEX INVERTERS

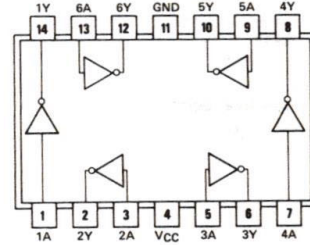
**04**

positive logic:  
 $Y = \overline{A}$

See page 6-2



SN5404 (J)      SN7404 (J, N)  
SN54H04 (J)    SN74H04 (J, N)  
SN54L04 (J)    SN74L04 (J, N)  
SN54LS04 (J, W) SN74LS04 (J, N)  
SN54S04 (J, W) SN74S04 (J, N)



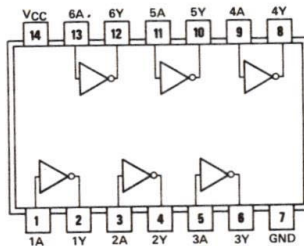
SN5404 (W)  
SN54H04 (W)  
SN54L04 (T)

HEX INVERTERS  
WITH OPEN-COLLECTOR OUTPUTS

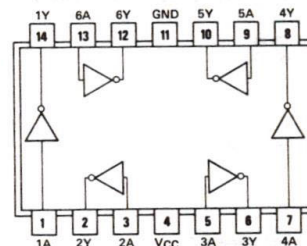
**05**

positive logic:  
 $Y = \overline{A}$

See page 6-4



SN5405 (J)      SN7405 (J, N)  
SN54H05 (J)    SN74H05 (J, N)  
SN54LS05 (J, W) SN74LS05 (J, N)  
SN54S05 (J, W) SN74S05 (J, N)



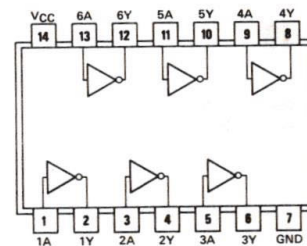
SN5405 (W)  
SN54H05 (W)

HEX INVERTER BUFFERS/DRIVERS  
WITH OPEN-COLLECTOR  
HIGH-VOLTAGE OUTPUTS

**06**

positive logic:  
 $Y = \overline{A}$

See page 6-24



SN5406 (J, W)    SN7406 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

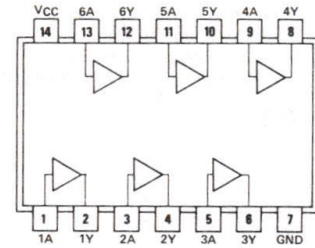
## PIN ASSIGNMENTS (TOP VIEWS)

HEX BUFFERS/DRIVERS  
WITH OPEN-COLLECTOR  
HIGH-VOLTAGE OUTPUTS

**07**

positive logic:  
 $Y = A$

See page 6-24



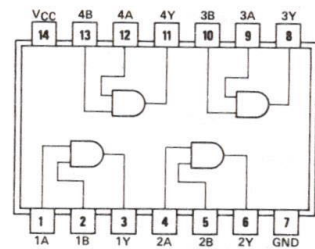
SN5407 (J, W) SN7407 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-AND GATES

**08**

positive logic:  
 $Y = AB$

See page 6-10



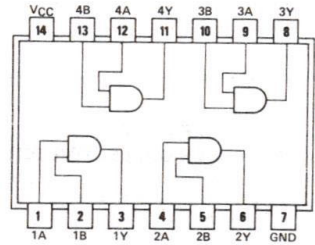
SN5408 (J, W) SN7408 (J, N)  
SN54LS08 (J, W) SN74LS08 (J, N)  
SN54S08 (J, W) SN74S08 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-AND GATES  
WITH OPEN-COLLECTOR OUTPUTS

**09**

positive logic:  
 $Y = AB$

See page 6-12



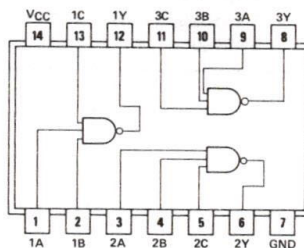
SN5409 (J, W) SN7409 (J, N)  
SN54LS09 (J, W) SN74LS09 (J, N)  
SN54S09 (J, W) SN74S09 (J, N)

TRIPLE 3-INPUT  
POSITIVE-NAND GATES

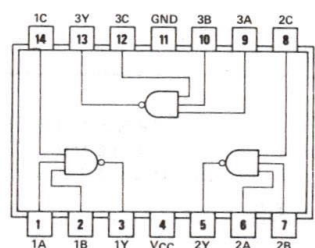
**10**

positive logic:  
 $Y = ABC$

See page 6-2



SN5410 (J) SN7410 (J, N)  
SN54H10 (J) SN74H10 (J, N)  
SN54L10 (J) SN74L10 (J, N)  
SN54LS10 (J, W) SN74LS10 (J, N)  
SN54S10 (J, W) SN74S10 (J, N)



SN5410 (W)  
SN54H10 (W)  
SN54L10 (T)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

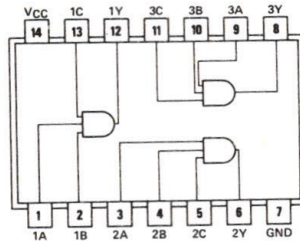
## PIN ASSIGNMENTS (TOP VIEWS)

### TRIPLE 3-INPUT POSITIVE-AND GATES

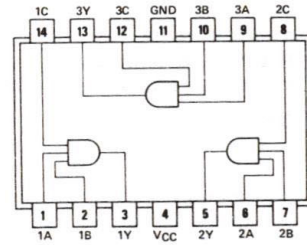
**11**

positive logic:  
 $Y = ABC$

See page 6-10



SN54H11 (J)      SN74H11 (J, N)  
SN54LS11 (J, W)    SN74LS11 (J, N)  
SN54S11 (J, W)    SN74S11 (J, N)



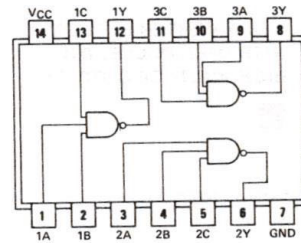
SN54H11 (W)

### TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

**12**

positive logic:  
 $Y = \overline{ABC}$

See page 6-4



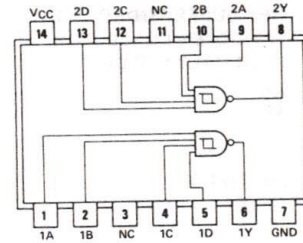
SN5412 (J, W)      SN7412 (J, N)  
SN54LS12 (J, W)    SN74LS12 (J, N)

### DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

**13**

positive logic:  
 $Y = \overline{ABCD}$

See page 6-14



SN5413 (J, W)      SN7413 (J, N)  
SN54LS13 (J, W)    SN74LS13 (J, N)

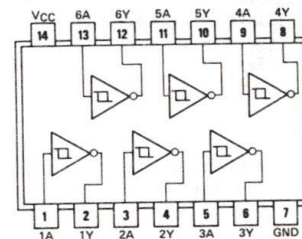
NC—No internal connection

### HEX SCHMITT-TRIGGER INVERTERS

**14**

positive logic:  
 $Y = \overline{A}$

See page 6-14



SN5414 (J, W)      SN7414 (J, N)  
SN54LS14 (J, W)    SN74LS14 (J, N)

5



# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

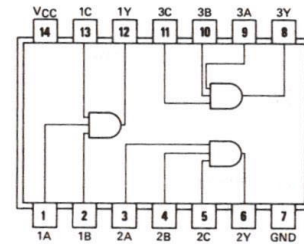
## PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT  
POSITIVE-AND GATES  
WITH OPEN-COLLECTOR OUTPUTS

**15**

positive logic:  
 $Y = ABC$

See page 6-12



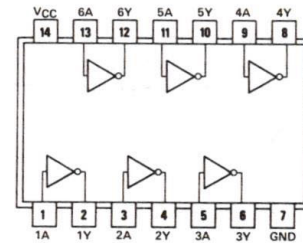
SN54H15 (J, W)      SN74H15 (J, N)  
SN54LS15 (J, W)    SN74LS15 (J, N)  
SN54S15 (J, W)      SN74S15 (J, N)

HEX INVERTER BUFFERS/DRIVERS  
WITH OPEN-COLLECTOR  
HIGH-VOLTAGE OUTPUTS

**16**

positive logic:  
 $Y = \bar{A}$

See page 6-24



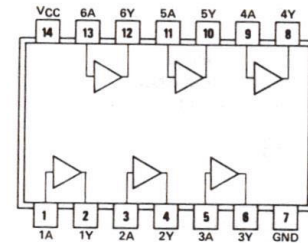
SN5416 (J, W)      SN7416 (J, N)

HEX BUFFERS/DRIVERS  
WITH OPEN-COLLECTOR  
HIGH-VOLTAGE OUTPUTS

**17**

positive logic:  
 $Y = A$

See page 6-24



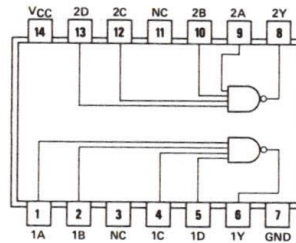
SN5417 (J, W)      SN7417 (J, N)

DUAL 4-INPUT  
POSITIVE-NAND GATES

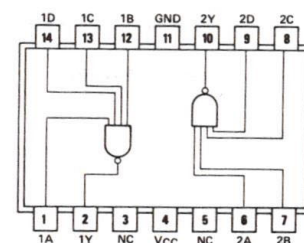
**20**

positive logic:  
 $Y = \overline{ABCD}$

See page 6-2



SN5420 (J)      SN7420 (J, N)  
SN54H20 (J)    SN74H20 (J, N)  
SN54L20 (J)    SN74L20 (J, N)  
SN54LS20 (J, W) SN74LS20 (J, N)  
SN54S20 (J, W) SN74S20 (J, N)



SN5420 (W)  
SN54H20 (W)  
SN54L20 (T)

NC—No internal connection

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

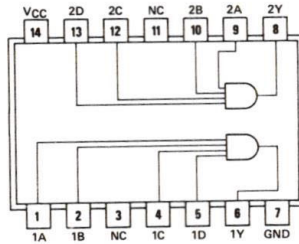
## PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-INPUT  
POSITIVE-AND GATES

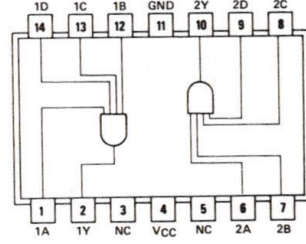
**21**

positive logic:  
 $Y = ABCD$

See page 6-10



SN54H21 (J) SN74H21 (J, N)  
SN54LS21 (J, W) SN74LS21 (J, N)



SN54H21 (W)

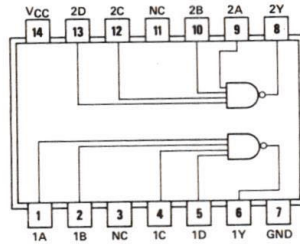
NC—No internal connection

DUAL 4-INPUT  
POSITIVE-NAND GATES  
WITH OPEN-COLLECTOR OUTPUTS

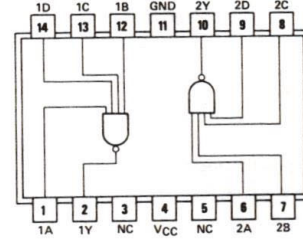
**22**

positive logic:  
 $Y = \overline{ABCD}$

See page 6-4



SN5422 (J, W) SN7422 (J, N)  
SN54H22 (J) SN74H22 (J, N)  
SN54LS22 (J, W) SN74LS22 (J, N)  
SN54S22 (J, W) SN74S22 (J, N)



SN54H22 (W)

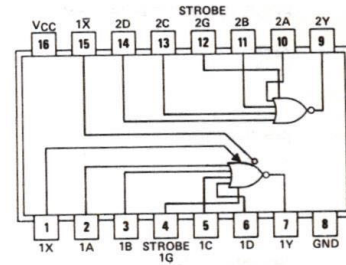
NC—No internal connection

EXPANDABLE DUAL 4-INPUT  
POSITIVE-NOR GATES  
WITH STROBE

**23**

positive logic:  
 $1Y = \overline{1G(1A+1B+1C+1D)+X}$   
 $2Y = \overline{2G(2A+2B+2C+2D)}$   
X = output of SN5460/SN7460

See page 6-39



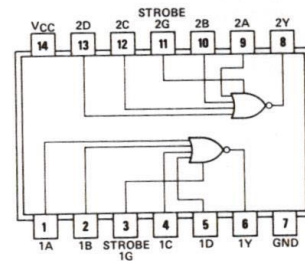
SN5423 (J, W) SN7423 (J, N)

DUAL 4-INPUT  
POSITIVE-NOR GATES  
WITH STROBE

**25**

positive logic:  
 $Y = \overline{G(A+B+C+D)}$

See page 6-8



SN5425 (J, W) SN7425 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

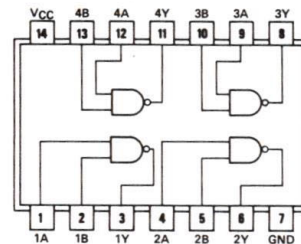
## PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT  
HIGH-VOLTAGE INTERFACE  
POSITIVE-NAND GATES

**26**

positive logic:  
 $Y = \overline{AB}$

See pages 6-24 and 6-26



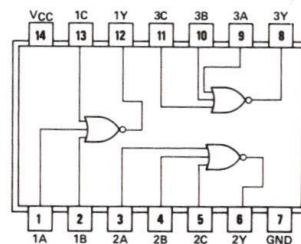
SN5426 (J) SN7426 (J, N)  
SN54LS26 (J, W) SN74LS26 (J, N)

TRIPLE 3-INPUT  
POSITIVE-NOR GATES

**27**

positive logic:  
 $Y = \overline{A+B+C}$

See page 6-8



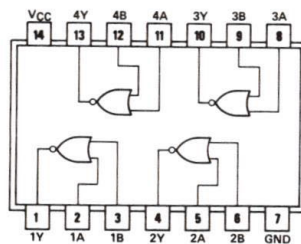
SN5427 (J, W) SN7427 (J, N)  
SN54LS27 (J, W) SN74LS27 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-NOR BUFFERS

**28**

positive logic:  
 $Y = \overline{A+B}$

See page 6-20



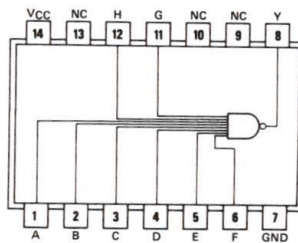
SN5428 (J, W) SN7428 (J, N)  
SN54LS28 (J, W) SN74LS28 (J, N)

8-INPUT  
POSITIVE-NAND GATES

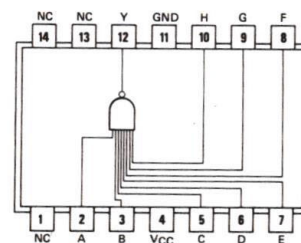
**30**

positive logic:  
 $Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J) SN7430 (J, N)  
SN54H30 (J) SN74H30 (J, N)  
SN54L30 (J) SN74L30 (J, N)  
SN54LS30 (J, W) SN74LS30 (J, N)  
SN54S30 (J, W) SN74S30 (J, N)



SN5430 (W)  
SN54H30 (W)  
SN54L30 (T)

NC—No internal connection

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

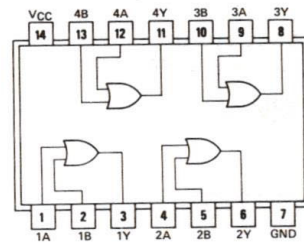
## PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT  
POSITIVE-OR GATES

**32**

positive logic:  
 $Y = A+B$

See page 6-28



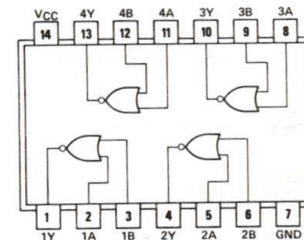
SN5432 (J, W)      SN7432 (J, N)  
SN54LS32 (J, W)    SN74LS32 (J, N)  
SN54S32 (J, W)    SN74S32 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-NOR BUFFERS  
WITH OPEN-COLLECTOR OUTPUTS

**33**

positive logic:  
 $Y = \overline{A+B}$

See pages 6-24 and 6-26



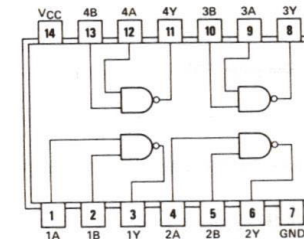
SN5433 (J, W)      SN7433 (J, N)  
SN54LS33 (J, W)    SN74LS33 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS

**37**

positive logic:  
 $Y = \overline{AB}$

See page 6-20



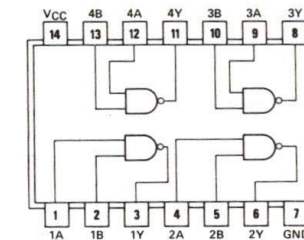
SN5437 (J, W)      SN7437 (J, N)  
SN54LS37 (J, W)    SN74LS37 (J, N)  
SN54S37 (J, W)      SN74S37 (J, N)

QUADRUPLE 2-INPUT  
POSITIVE-NAND BUFFERS  
WITH OPEN-COLLECTOR OUTPUTS

**38**

positive logic:  
 $Y = \overline{AB}$

See pages 6-24 and 6-26



SN5438 (J, W)      SN7438 (J, N)  
SN54LS38 (J, W)    SN74LS38 (J, N)  
SN54S38 (J, W)      SN74S38 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

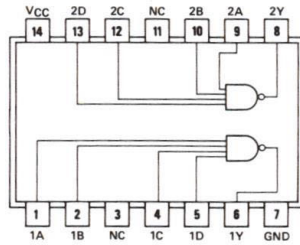
## PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-INPUT  
POSITIVE-NAND BUFFERS

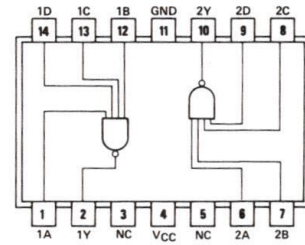
**40**

positive logic:  
 $Y = ABCD$

See page 6-20



SN5440 (J)      SN7440 (J, N)  
SN54H40 (J)    SN74H40 (J, N)  
SN54LS40 (J,W) SN74LS40 (J, N)  
SN54S40 (J, W) SN74S40 (J, N)



SN5440 (W)  
SN54H40 (W)

NC—No internal connection

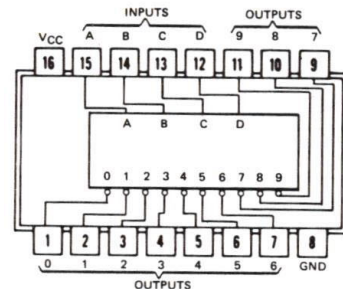
4 LINE-TO-10-LINE DECODERS

**42** BCD-TO-DECIMAL

**43** EXCESS-3-TO-DECIMAL

**44** EXCESS-3-GRAY-TO-DECIMAL

See page 7-15

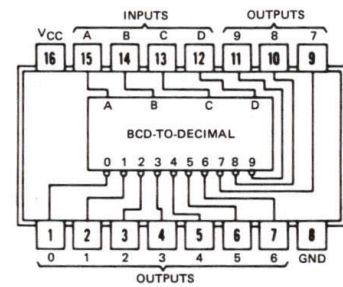


SN5442A (J, W)    SN7442A (J, N)  
SN54L42 (J)      SN74L42 (J, N)  
SN54LS42 (J, W) SN74LS42 (J, N)  
SN5443A (J, W)    SN7443A (J, N)  
SN54L43 (J)      SN74L43 (J, N)  
SN5444A (J, W)    SN7444A (J, N)  
SN54L44 (J)      SN74L44 (J, N)

BCD-TO-DECIMAL DECODER/DRIVER

**45** LAMP, RELAY, OR MOS DRIVER  
80-mA CURRENT SINK  
OUTPUTS OFF FOR INVALID CODES

See page 7-20



SN5445 (J, W)    SN7445 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

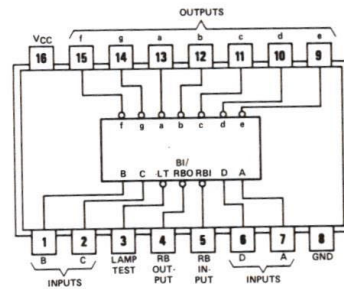
## PIN ASSIGNMENTS (TOP VIEWS)

### BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**46** ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

**47** ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS

See page 7-22

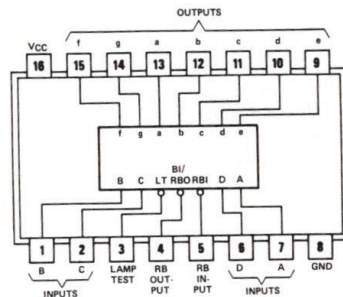


SN5446A (J, W)	SN7446A (J, N)
SN54L46 (J)	SN74L46 (J, N)
SN5447A (J, W)	SN7447A (J, N)
SN54L47 (J)	SN74L47 (J, N)
SN54LS47 (J, W)	SN74LS47 (J, N)

### BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**48** INTERNAL PULL-UP OUTPUTS

See page 7-22

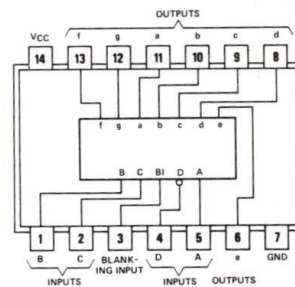


SN5448 (J, W)	SN7448 (J, N)
SN54LS48 (J, W)	SN74LS48 (J, N)

### BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**49** OPEN-COLLECTOR OUTPUTS

See page 7-22



SN5449 (W)	
SN54LS49 (J, W)	SN74LS49 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

DUAL 2-WIDE 2-INPUT  
AND-OR-INVERT GATES  
(ONE GATE EXPANDABLE)

**50**

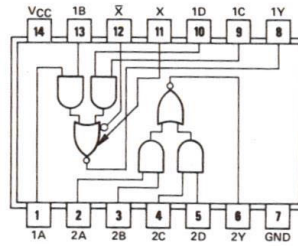
positive logic:

$$Y = \overline{AB} + CD + X$$

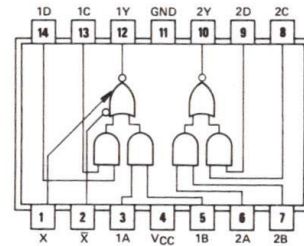
'50: X = output of SN5460/SN7460

'H50: X = output of SN54H60/SN74H60  
or SN54H62/SN74H62

See page 6-39



SN5450 (J)      SN7450 (J, N)  
SN54H50 (J)    SN74H50 (J, N)



SN5450 (W)  
SN54H50 (W)

AND-OR-INVERT GATES

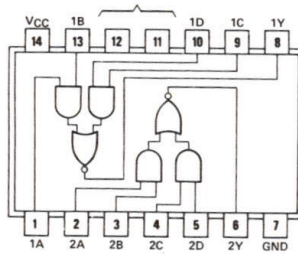
**51**

'51, 'H51, 'S51  
DUAL 2-WIDE 2-INPUT

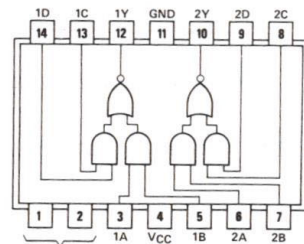
positive logic:

$$Y = \overline{AB} + CD$$

MAKE NO EXTERNAL CONNECTION



SN5451 (J)      SN7451 (J, N)  
SN54H51 (J)    SN74H51 (J, N)  
SN54S51 (J, W) SN74S51 (J, N)



MAKE NO EXTERNAL CONNECTION

SN5451 (W)  
SN54H51 (W)

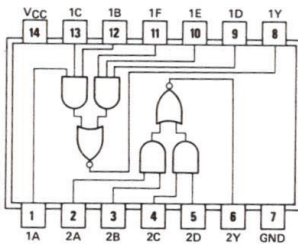
'L51, 'LS51  
2-WIDE 3-INPUT,  
2-WIDE 2-INPUT

positive logic:

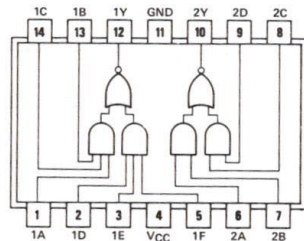
$$1Y = \overline{(1A \cdot 1B \cdot 1C)} + (1D \cdot 1E \cdot 1F)$$

$$2Y = \overline{(2A \cdot 2B)} + (2C \cdot 2D)$$

See page 6-30



SN54L51 (J)      SN74L51 (J, N)  
SN54LS51 (J, W) SN74LS51 (J, N)



SN54L51 (T)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### EXPANDABLE 4-WIDE AND-OR GATES

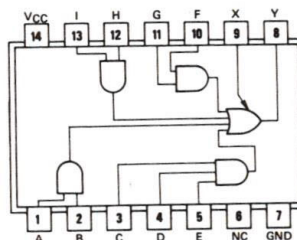
#### 52

'H52(J, N)

positive logic:

$$Y = AB + CDE + FG + HI + X$$

X = output of SN54H61/SN74H61



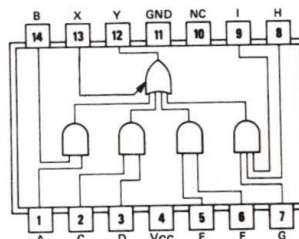
SN54H52 (J) SN74H52 (J, N)

'H52(W)

positive logic:

$$Y = AB + CD + EF + GH + X$$

X = output of SN54H61/SN74H61



SN54H52 (W)

See page 6-39

NC—No internal connection

### EXPANDABLE 4-WIDE AND-OR-INVERT GATES

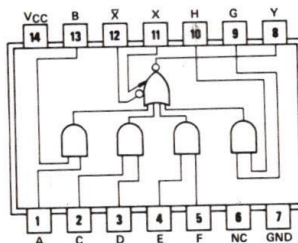
#### 53

'53

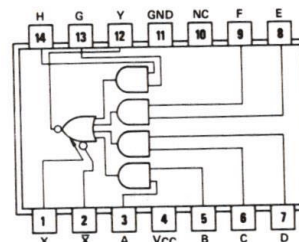
positive logic:

$$Y = \overline{AB + CD + EF + GH + X}$$

X = output of SN5460/SN7460



SN5453 (J) SN7453 (J, N)



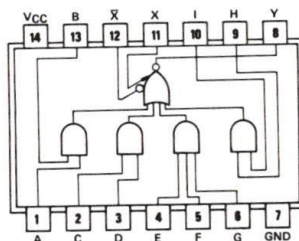
SN5453 (W)

'H53

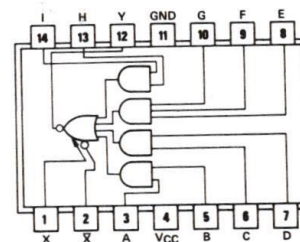
positive logic:

$$Y = \overline{AB + CD + EFG + HI + X}$$

X = output of SN54H60/SN74H60 or SN54H62/SN74H62



SN54H53 (J) SN74H53 (J, N)



SN54H53 (W)

See page 6-39

NC—No internal connection



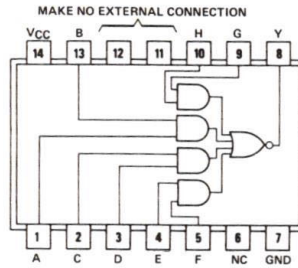
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

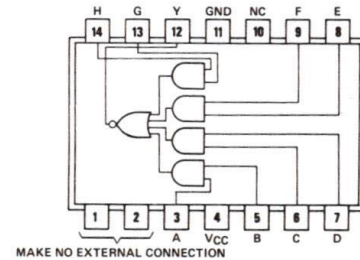
4-WIDE  
AND-OR-INVERT GATES

**54**

'54  
positive logic:  
 $Y = \overline{AB+CD+EF+GH}$

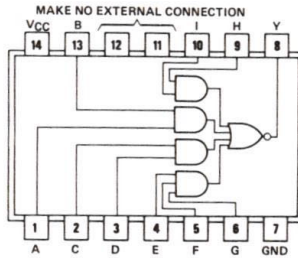


SN5454 (J) SN7454 (J, N)

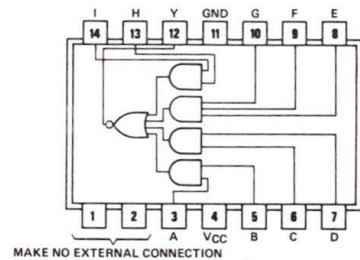


SN5454 (W)

'H54  
positive logic:  
 $Y = \overline{AB+CD+EFG+HI}$

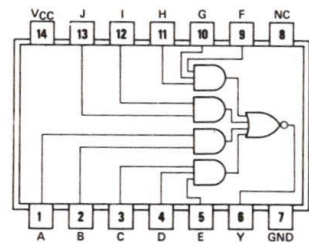


SN54H54 (J) SN74H54 (J, N)



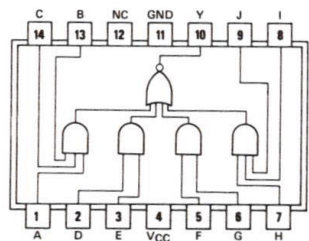
SN54H54 (W)

'L54(J, N), 'LS54  
positive logic:  
 $Y = \overline{AB+CDE+FGH+IJ}$



SN54L54 (J) SN74L54 (J, N)  
SN54LS54 (J, W) SN74LS54 (J, N)

'L54(T)  
positive logic:  
 $Y = \overline{ABC+DE+FG+HIJ}$



SN54L54 (T)

See page 6-30

NC—No internal connection

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 2-WIDE 4-INPUT AND-OR-INVERT GATES

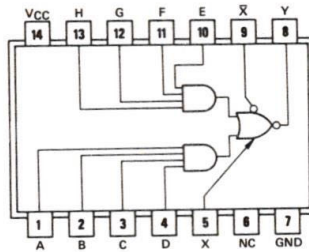
#### 55

'H55 (EXPANDABLE)  
positive logic:

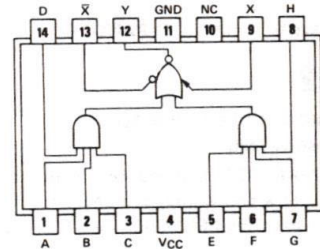
$$Y = \overline{ABCD + EFGH + X}$$

X = output of SN54H60/SN74H60  
or SN54H62/SN74H62

See page 6-39



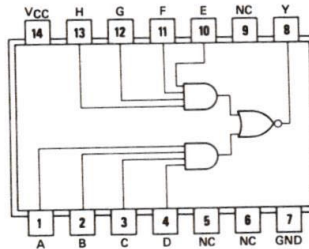
SN54H55 (J) SN74H55 (J, N)



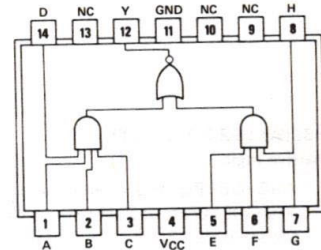
SN54H55 (W)

'L55, 'LS55  
positive logic:  
 $Y = \overline{ABCD + EFGH}$

See page 6-30



SN54L55 (J) SN74L55 (J, N)  
SN54LS55 (J, W) SN74LS55 (J, N)



SN54L55 (T)  
NC—No internal connection

### DUAL 4-INPUT EXPANDERS

#### 60

positive logic:

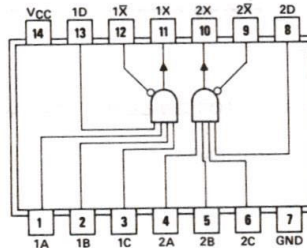
X = ABCD when connected to X and  $\bar{X}$  inputs  
of SN5423/SN7423, SN5450/SN7450, or  
SN5453/SN7453

'H60

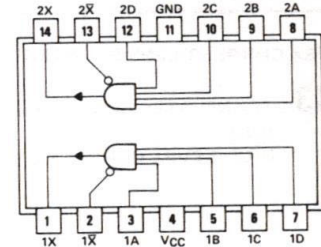
positive logic:

X = ABCD when connected to X and  $\bar{X}$   
inputs of SN54H50/SN74H50,  
SN54H53/SN74H53, or  
SN54H55/SN74H55

See pages 6-43 and 6-44



SN5460 (J) SN7460 (J, N)  
SN54H60 (J) SN74H60 (J, N)



SN5460 (W)  
SN54H60 (W)

NC—No internal connection

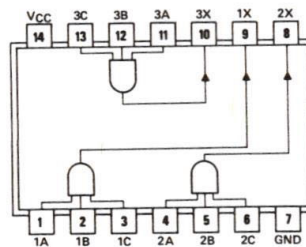
### TRIPLE 3-INPUT EXPANDERS

#### 61

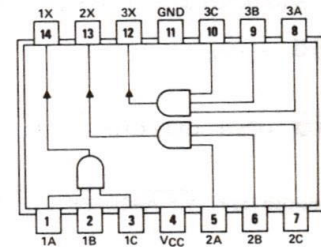
positive logic:

X = ABC when connected to X input of  
SN54H52/SN74H52

See page 6-45



SN54H61 (J) SN74H61 (J, N)



SN54H61 (W)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

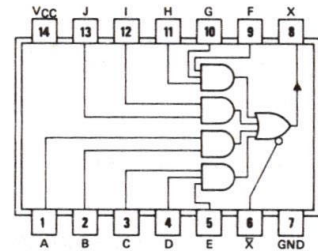
### 4-WIDE AND-OR EXPANDERS

#### 62

'H62(J, N) (2-3-3-2 INPUT)

positive logic:

$X = AB + CDE + FGH + IJ$  when connected to X and  $\bar{X}$  inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

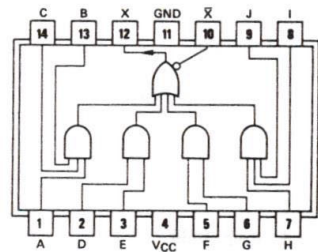


SN54H62 (J) SN74H62 (J, N)

'H62(W) (3-2-2-3 INPUT)

positive logic:

$X = ABC + DE + FG + HIJ$  when connected to X and  $\bar{X}$  inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55



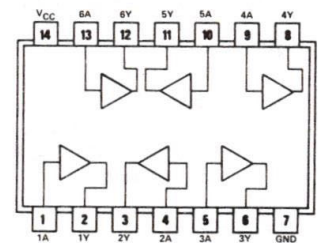
SN54H62 (W)

See page 6-44

### HEX CURRENT-SENSING INTERFACE GATES

#### 63

TRANSLATES LOW-LEVEL INPUT CURRENT TO LOW-LEVEL VOLTAGE AND HIGH-LEVEL CURRENT TO HIGH-LEVEL VOLTAGE



SN54LS63(J,W) SN74LS63(J,N)

See page 6-62

### 4-2-3-2 INPUT AND-OR-INVERT GATES

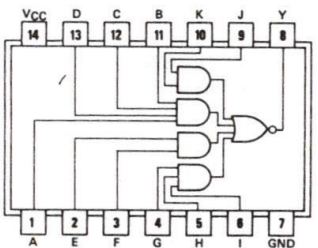
#### 64

TOTEM-POLE OUTPUT

#### 65

OPEN-COLLECTOR OUTPUT

positive logic:  $\bar{Y} = ABCD + EF + GHI + JK$



SN54S64 (J, W) SN74S64 (J, N)  
SN54S65 (J, W) SN74S65 (J, N)

See pages 6-30 and 6-32

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**70**

#### FUNCTION TABLE

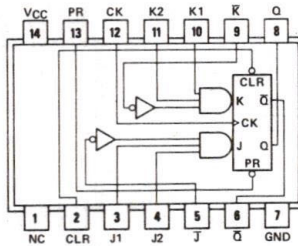
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↑	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}_0$

positive logic:  $J = J1 \cdot J2 \cdot \bar{J}$

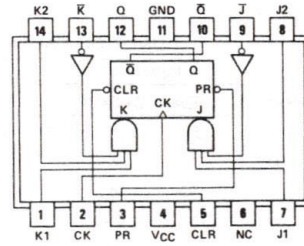
$K = K1 \cdot K2 \cdot \bar{K}$

If inputs J and  $\bar{K}$  are not used, they must be grounded.

See page 6-46 Preset or clear function can occur only when the clock input is low.



SN5470 (J) SN7470 (J, N)



SN5470 (W)

NC—No internal connection

### AND-OR-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

**H71**

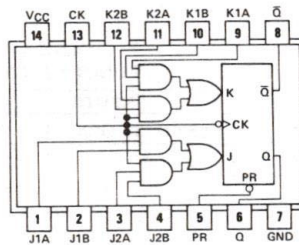
#### FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

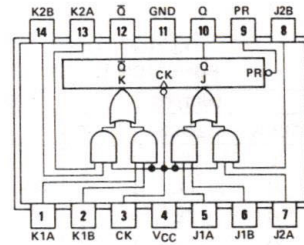
positive logic:  $J = (J1A \cdot J1B) + (J2A \cdot J2B)$

$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

See page 6-50



SN54H71 (J) SN74H71 (J, N)



SN54H71 (W)

### AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

**L71**

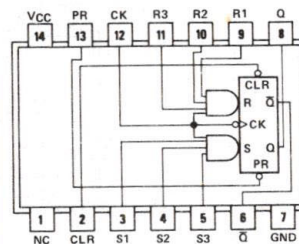
#### FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	INDETERMINATE	

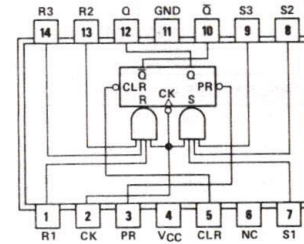
positive logic:  $R = R1 \cdot R2 \cdot R3$

$S = S1 \cdot S2 \cdot S3$

See page 6-54



SN54L71 (J) SN74L71 (J, N)



SN54L71 (T)

NC—No internal connection

See explanation of function tables on page 3-8.

\* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

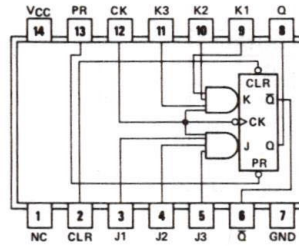
**72**

FUNCTION TABLE

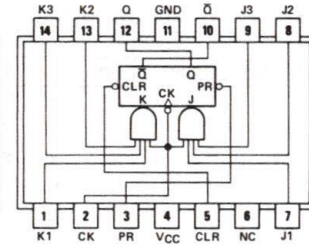
INPUTS			OUTPUTS			
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\uparrow$	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	$\uparrow$	H	L	H	L
H	H	$\uparrow$	L	H	L	H
H	H	$\uparrow$	H	H	TOGGLE	

positive logic: J = J1·J2·J3; K1·K2·K3

See pages 6-46, 6-50, and 6-54



SN5472 (J) SN7472 (J, N)  
 SN54H72 (J) SN74H72 (J, N)  
 SN54L72 (J) SN74L72 (J, N)



SN5472 (W) SN54H72 (W)  
 SN54L72 (T)

NC—No internal connection

### DUAL J-K FLIP-FLOPS WITH CLEAR

**73**

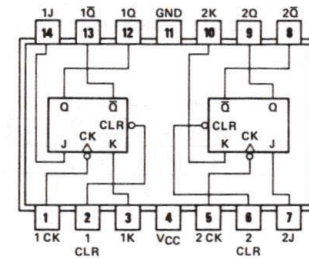
'73, 'H73, 'L73  
FUNCTION TABLE

INPUTS			OUTPUTS		
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\uparrow$	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	$\uparrow$	H	L	H	L
H	$\uparrow$	L	H	L	H
H	$\uparrow$	H	H	TOGGLE	

'LS73A  
FUNCTION TABLE

INPUTS			OUTPUTS		
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5473 (J, W) SN7473 (J, N)  
 SN54H73 (J, W) SN74H73 (J, N)  
 SN54L73 (J, T) SN74L73 (J, N)  
 SN54LS73A (J, W) SN74LS73A (J, N)

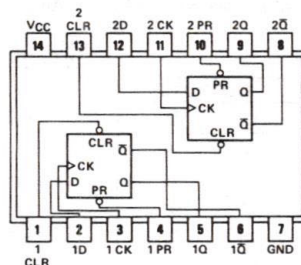
### DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**74**

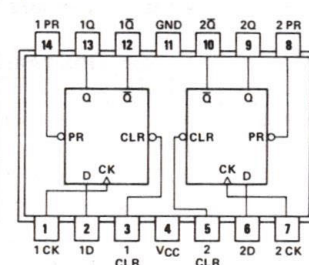
FUNCTION TABLE

INPUTS			OUTPUTS		
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	$\uparrow$	L	Q <sub>0</sub>	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56



SN5474 (J) SN7474 (J, N)  
 SN54H74 (J) SN74H74 (J, N)  
 SN54L74 (J) SN74L74 (J, N)  
 SN54LS74A (J, W) SN74LS74A (J, N)  
 SN54S74 (J, W) SN74S74 (J, N)



SN5474 (W) SN54H74 (W)  
 SN54L74 (T)

See explanation of function tables on page 3-8.

\*This configuration is nonstable; that is, it will not persist when preset or clear inputs return to their inactive (high) level. Furthermore, the output levels of the 'LS74A in this configuration are not guaranteed to meet the minimum levels for V<sub>OH</sub> if the lows at preset and clear are near V<sub>IL</sub> maximum.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT BISTABLE LATCHES

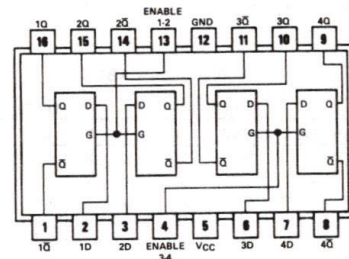
# 75

FUNCTION TABLE  
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q <sub>0</sub>	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant  
Q<sub>0</sub> = the level of Q before the high-to-low transition of G

See page 7-35



SN5475 (J, W) SN7475 (J, N)  
SN54L75 (J) SN74L75 (J, N)  
SN54LS75 (J, W) SN74LS75 (J, N)

### DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

# 76

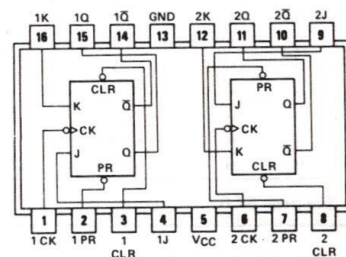
'76, 'H76  
FUNCTION TABLE

INPUTS				OUTPUTS		
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\downarrow$	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	TOGGLE	TOGGLE

'LS76A  
FUNCTION TABLE

INPUTS				OUTPUTS		
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\downarrow$	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	$\downarrow$	H	L	H	L
H	H	$\downarrow$	L	H	L	H
H	H	$\downarrow$	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

See pages 6-46, 6-50, and 6-56



SN5476 (J, W) SN7476 (J, N)  
SN54H76 (J, W) SN74H76 (J, N)  
SN54LS76A (J, W) SN74LS76A (J, N)

### 4-BIT BISTABLE LATCHES

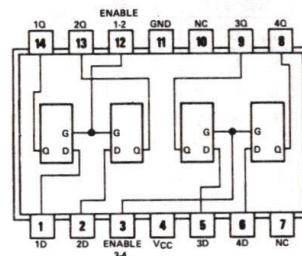
# 77

FUNCTION TABLE  
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q <sub>0</sub>	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant  
Q<sub>0</sub> = the level of Q before the high-to-low transition of G

See page 7-35



SN5477 (W)  
SN54L77 (T)  
SN54LS77 (W)

See explanation of function tables on page 3-8.

\*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

**78** 'H78, 'L78  
FUNCTION TABLE

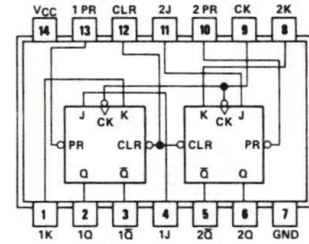
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	$\square$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\square$	H	L	H	L
H	H	$\square$	L	H	L	H
H	H	$\square$	H	H	TOGGLE	TOGGLE

See pages 6-50 and 6-54

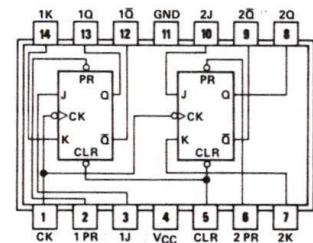
'LS78A  
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	I	L	L	$Q_0$	$\bar{Q}_0$
H	H	I	H	L	H	L
H	H	I	L	H	L	H
H	H	I	H	H	TOGGLE	TOGGLE
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

See page 6-56



SN54H78(J,W) SN74H78(J,N)



SN54L78(J,T) SN74L78(J,N)  
SN54LS78A(J,W) SN74LS78A(J,N)

### GATED FULL ADDERS

**80** GATED COMPLEMENTARY INPUTS  
COMPLEMENTARY SUM OUTPUTS

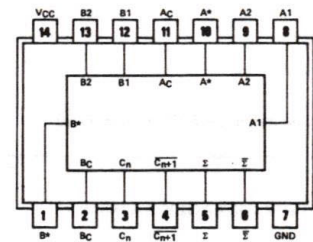
FUNCTION TABLE  
(See Notes 1, 2, and 3)

INPUTS			OUTPUTS		
$C_n$	B	A	$\bar{C}_{n+1}$	$\bar{\Sigma}$	$\Sigma$
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

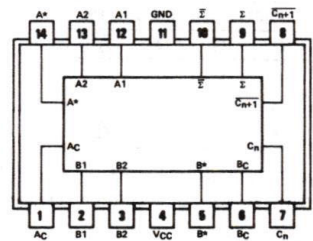
H = high level, L = low level

- NOTES: 1.  $A = \bar{A}_c + \bar{A}^* + A1 \cdot A2$ ,  $B = \bar{B}_c + B^* + B1 \cdot B2$ .  
 2. When  $A^*$  is used as an input,  $A1$  or  $A2$  must be low. When  $B^*$  is used as an input,  $B1$  or  $B2$  must be low.  
 3. When  $A1$  and  $A2$  or  $B1$  and  $B2$  are used as inputs,  $A^*$  or  $B^*$ , respectively, must be open or used to perform dot-AND logic.

See page 7-41



SN5480(J) SN7480(J,N)



SN5480(W)

See explanation of function tables on page 3-8.

\*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

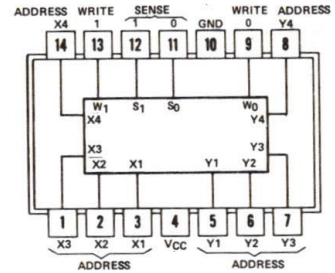
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

16-BIT RANDOM-ACCESS MEMORIES

**81**

See page 7-44

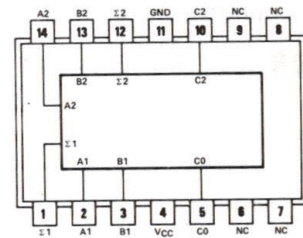


SN5481A (J, W) SN7481A (J, N)

2-BIT BINARY FULL ADDERS

**82**

See page 7-49



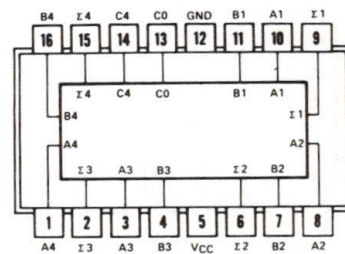
SN5482 (J, W) SN7482 (J, N)

NC—No internal connection

4-BIT BINARY FULL ADDERS WITH FAST CARRY

**83**

See page 7-53

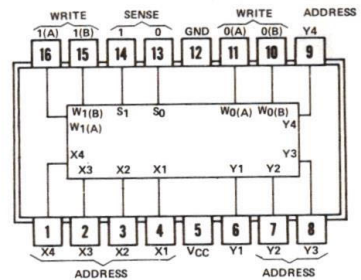


SN5483A (J, W) SN74 83A (J, N)  
SN54LS83A (J, W) SN74LS83A (J, N)

16-BIT RANDOM-ACCESS MEMORIES

**84**

See page 7-44



SN5484A (J, W) SN7484A (J, N)

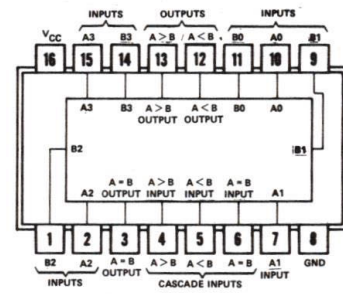
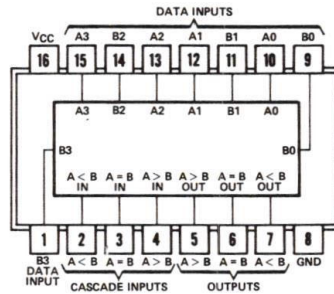


# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT MAGNITUDE COMPARATORS

**85**



SN5485 (J, W) SN7485 (J, N)  
 SN54LS85 (J, W) SN74LS85 (J, N)  
 SN54S85 (J, W) SN74S85 (J, N)

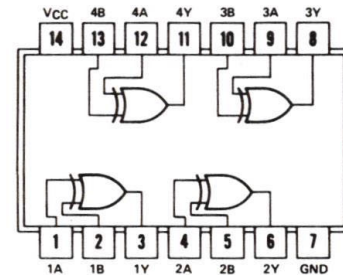
SN54L85 (J) SN74L85 (J, N)

See page 7-57

### QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

**86**

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

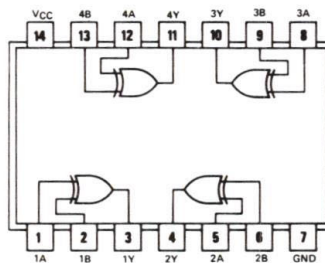


SN5486 (J, W) SN7486 (J, N)  
 SN54LS86 (J, W) SN74LS86 (J, N)  
 SN54S86 (J, W) SN74S86 (J, N)

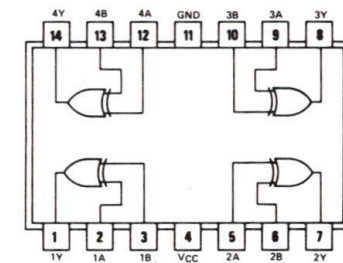
#### FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



SN54L86 (J) SN74L86 (J, N)



SN54L86 (T)

See page 7-65

### 4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENTS

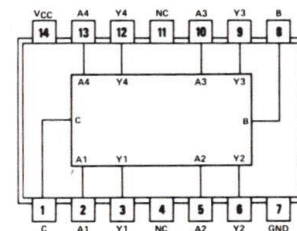
**87**

#### FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\bar{A}1$	$\bar{A}2$	$\bar{A}3$	$\bar{A}4$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level

A1, A2, A3, A4 = the level of the respective A input



SN54H87 (J, W) SN74H87 (J, N)

NC—No internal connection

See page 7-70

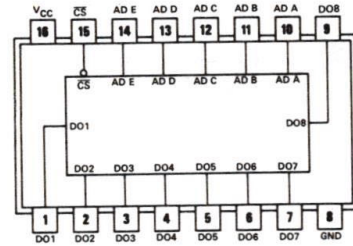
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 256-BIT READ-ONLY MEMORIES

**88** 32 8-BIT WORDS  
OPEN-COLLECTOR OUTPUTS

For more information contact the factory

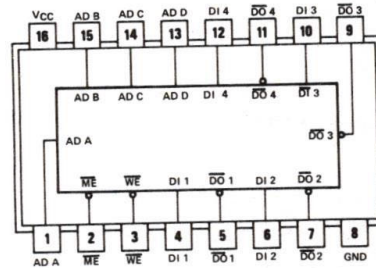


SN5488A (J, W) SN7488A (J, N)

### 64-BIT READ/WRITE MEMORIES

**89** 16 4-BIT WORDS

For more information contact the factory

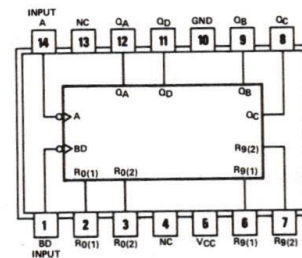


SN7489 (J, N)

### DECADE COUNTERS

**90** DIVIDE-BY-TWO AND DIVIDE-BY FIVE

See Page 7-72



SN5490A (J, W) SN7490A (J, N)  
SN54L90 (J, T) SN74L90 (J, N)  
SN54LS90 (J, W) SN74LS90 (J, N)

NC - No internal connection

5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 8-BIT SHIFT REGISTERS

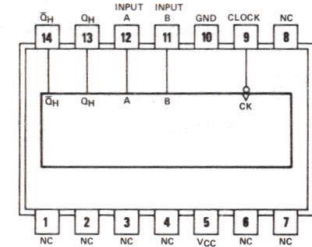
**91** SERIAL-IN, SERIAL-OUT  
GATED INPUT

FUNCTION TABLE

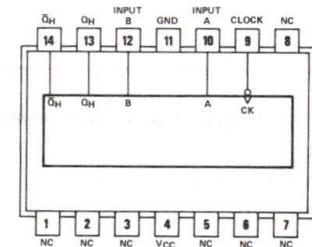
INPUTS AT $t_n$		OUTPUTS AT $t_{n+8}$	
A	B	$Q_H$	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

See Page 7-81

H = high, L = low  
X = irrelevant  
 $t_n$  = Reference bit time, clock low  
 $t_{n+8}$  = Bit time after 8 low-to-high clock transitions



SN5491A (J)      SN7491A (J,N)  
SN54L91 (J)      SN74L91 (J, N)  
SN54LS91 (J)      SN74LS91 (J, N)



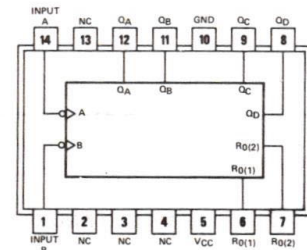
SN5491A (W)  
SN54L91 (T)  
SN54LS91 (W)

NC — No internal connections

### DIVIDE-BY-TWELVE COUNTERS

**92** DIVIDE-BY-TWO AND DIVIDE-BY-SIX

See Page 7-72



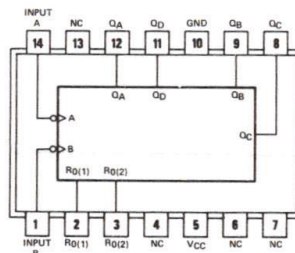
SN5492A (J, W)      SN7492A (J, N)  
SN54LS92 (J, W)      SN74LS92 (J, N)

NC—No internal connection

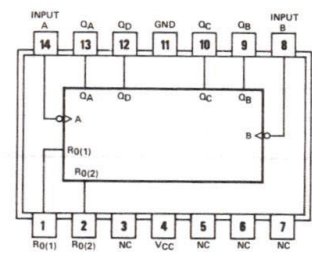
### 4-BIT BINARY COUNTERS

**93** DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT

See Page 7-72



SN5493A (J, W)      SN7493A (J, N)  
SN54LS93 (J, W)      SN74LS93 (J, N)



SN54L93 (J, T)      SN74L93 (J, N)

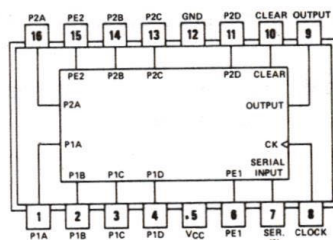
NC—No internal connection

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT SHIFT REGISTERS

#### 94 DUAL ASYNCHRONOUS PRESETS

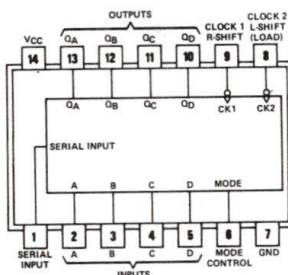


SN5494 (J, W) SN7494 (J, N)

See Page 7-86

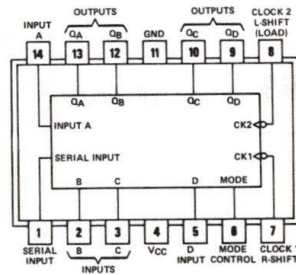
### 4-BIT SHIFT REGISTERS

#### 95 PARALLEL IN/PARALLEL OUT SHIFT RIGHT, SHIFT LEFT SERIAL INPUT



SN5495A (J, W) SN7495A (J, N)  
SN54LS95B (J, W) SN74LS95B (J, N)

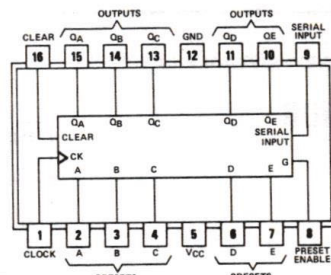
See Page 7-89



SN54L95 (J, T) SN74L95 (J, N)

### 5-BIT SHIFT REGISTERS

#### 96 ASYNCHRONOUS PRESET

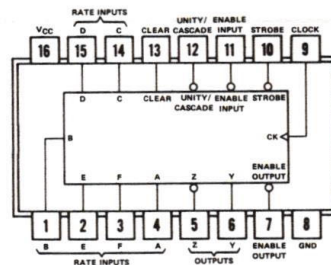


SN5496 (J, W) SN7496 (J, N)  
SN54L96 (J) SN74L96 (J, N)  
SN54LS96 (J, W) SN74LS96 (J, N)

See Page 7-95

### SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

#### 97



SN5497 (J, W) SN7497 (J, N)

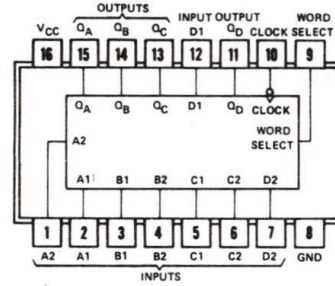
See Page 7-102

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT DATA SELECTOR/STORAGE REGISTERS

**98** SELECTS 1 OF 2 4-BIT WORDS  
PARALLEL IN/OUT

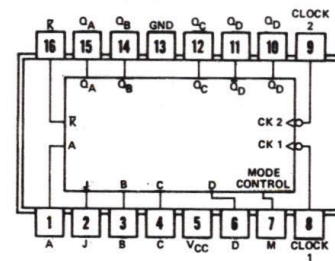


SN54L98 (J) SN74L98 (J, N)

See Page 7-107

### 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

**99** SERIAL J-K INPUTS



SN54L99 (J) SN74L99 (J, N)

See Page 7-109

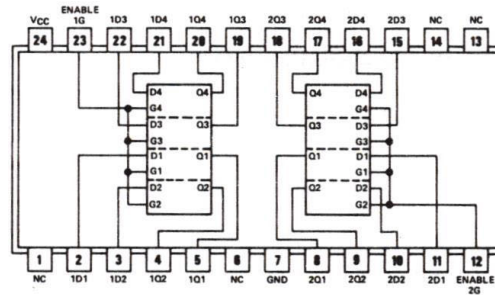
### 8-BIT BISTABLE LATCHES

**100**

FUNCTION TABLE  
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	$Q_0$	$\bar{Q}_0$

H = high level, X = irrelevant  
 $Q_0$  = the level of Q before the high-to-low transition of G



SN54100 (J, W) SN74100 (J, N)

NC — No internal connection

See Page 7-113

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

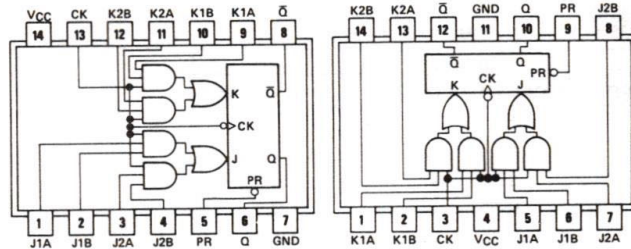
**101**

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

positive logic:  $J = (J1A \cdot J1B) + (J2A \cdot J2B)$   
 $K = (K1A \cdot K1B) + (K2A \cdot K2B)$

See page 6-52



SN54H101 (J) SN74H101 (J, N) SN54H101 (W)

### AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

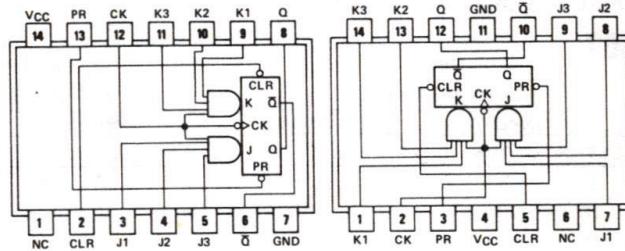
**102**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

positive logic:  $J = J1 \cdot J2 \cdot J3$   
 $K = K1 \cdot K2 \cdot K3$

See page 6-52



SN54H102 (J) SN74H102 (J,N) SN54H102 (W)

NC—No internal connection

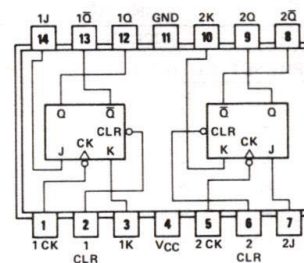
### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

**103**

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

See page 6-52



SN54H103 (J, W) SN74H103 (J, N)

See explanation of function tables on page 3-8.

\*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

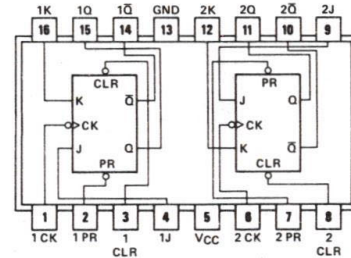
## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**106**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54H106 (J, W) SN74H106 (J, N)

See page 6-52

### DUAL J-K FLIP-FLOPS WITH CLEAR

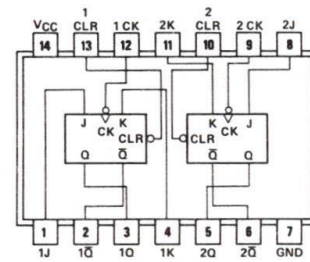
**107**

'107  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

'LS107A  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54107 (J) SN74107 (J, N)  
SN54LS107A (J) SN74LS107A (J, N)

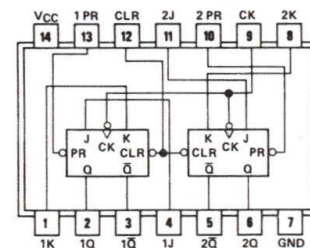
See pages 6-46 and 6-56

### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

**108**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54H108 (J, W) SN74H108 (J, N)

See page 6-52

See explanation of function tables on page 3-8.

\*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

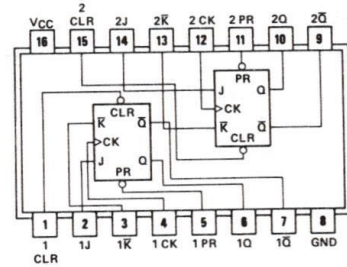
### DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**109**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

See pages 6-46 and 6-56



SN54109 (J, W)      SN74109 (J, N)  
SN54LS109A (J, W)      SN74LS109A (J, N)

### AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

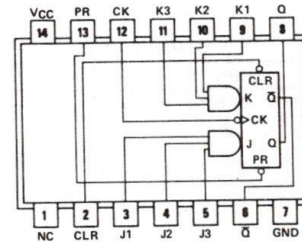
**110**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

positive logic: J = J1·J2·J3  
K = K1·K2·K3

See page 6-46



SN54110 (J, W)      SN74110 (J, N)

NC—No internal connection

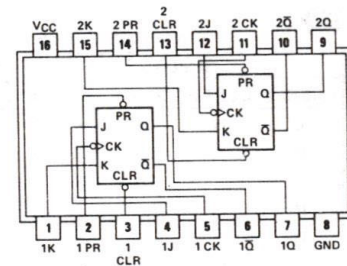
### DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

**111**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

See page 6-46



SN54111 (J, W)      SN74111 (J, N)

See explanation of function tables on page 3-8.

\* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

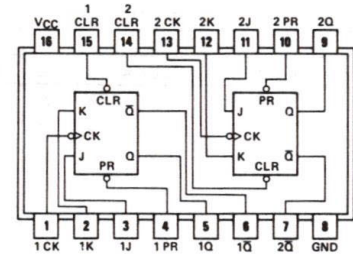
## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

**112**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54LS112A (J, W) SN74LS112A (J, N)  
SN54S112 (J, W) SN74S112 (J, N)

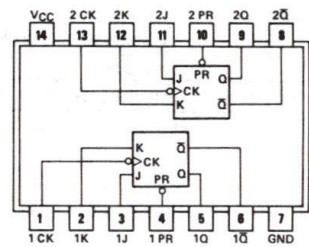
See pages 6-56 and 6-58

### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

**113**

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54LS113A (J, W) SN74LS113A (J, N)  
SN54S113 (J, W) SN74S113 (J, N)

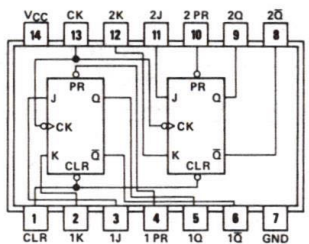
See pages 6-56 and 6-58

### DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

**114**

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>



SN54LS114A (J, W) SN74LS114A (J, N)  
SN54S114 (J, W) SN74S114 (J, N)

See pages 6-56 and 6-58

See explanation of function tables on page 3-8.

\* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

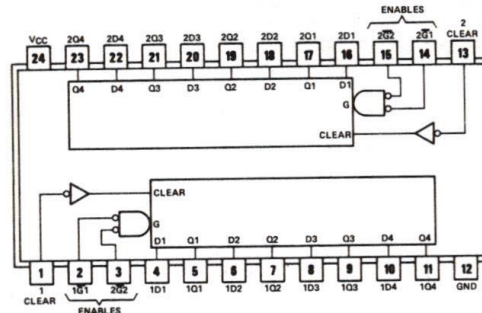
## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL 4-BIT LATCHES

116

FUNCTION TABLE  
(EACH LATCH)

CLEAR	ENABLES		DATA	OUTPUT Q
	$\overline{G1}$	$\overline{G2}$		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	$Q_0$
H	H	X	X	$Q_0$
L	X	X	X	L



SN54116 (J, W) SN74116 (J, N)

See page 7-115

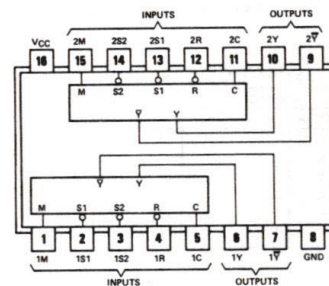
### DUAL PULSE SYNCHRONIZERS/DRIVERS

120

FUNCTION TABLE

R	INPUTS		FUNCTION
	S1	S2	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

†Operation initiated by last ↓ transition continues.



SN54120 (J, W) SN74120 (J, N)

See page 7-118

### MONOSTABLE MULTIVIBRATORS

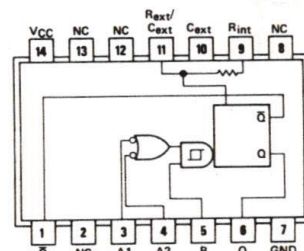
121

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L*	H*
X	X	L	L*	H*
H	H	X	L*	H*
H	↓	H	⌋	⌋
↓	H	H	⌋	⌋
↓	↓	H	⌋	⌋
L	X	↑	⌋	⌋
X	L	↑	⌋	⌋

See page 6-64

- NOTES: 1. An external capacitor may be connected between  $C_{ext}$  (positive) and  $R_{ext}/C_{ext}$ .
2. To use the internal timing resistor, connect  $R_{int}$  to  $V_{CC}$ . For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.



SN54121 (J, W) SN74121 (J, N)  
SN54L121 (J, T) SN74L121 (J, N)  
\*121 ...  $R_{int} = 2 \text{ k}\Omega \text{ NOM}$   
\*L121 ...  $R_{int} = 4 \text{ k}\Omega \text{ NOM}$

NC—No internal connection

See explanation of function tables on page 3-8.

\*These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

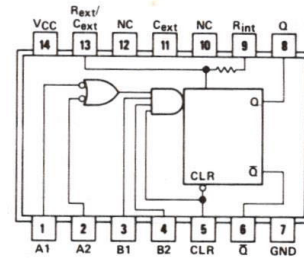
### RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

#### 122 FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L*	H*
X	X	X	L	X	L*	H*
X	X	X	X	L	L*	H*
H	L	X	†	H		
H	L	X	H	†		
H	X	L	†	H		
H	X	L	H	†		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
†	L	X	H	H		
†	X	L	H	H		

- NOTES: 1. An external timing capacitor may be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive).  
 2. For accurate repeatable pulse widths, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.

See page 6-76



SN54122 (J, W) SN74122 (J, N)  
 SN54L122 (J, T) SN74L122 (J, N)  
 SN54LS122 (J, W) SN74LS122 (J, N)  
 \*122 ...  $R_{int} = 10 \text{ k}\Omega \text{ NOM}$   
 \*L122 ...  $R_{int} = 20 \text{ k}\Omega \text{ NOM}$   
 \*LS122 ...  $R_{int} = 10 \text{ k}\Omega \text{ NOM}$

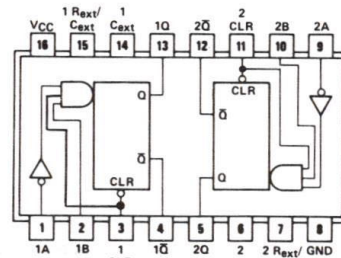
NC—No internal connection

### DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

#### 123 FUNCTION TABLE

CLEAR	INPUTS		OUTPUTS	
	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L*	H*
X	X	L	L*	H*
H	L	†		
H	↓	H		
†	L	H		

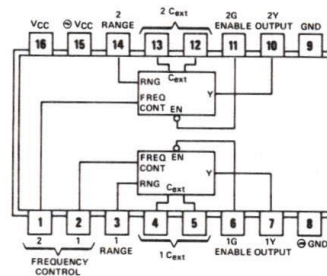
See page 6-76



SN54123 (J, W) SN74123 (J, N)  
 SN54L123 (J) SN74L123 (J, N)  
 SN54LS123 (J, W) SN74LS123 (J, N)

### DUAL VOLTAGE-CONTROLLED OSCILLATORS

#### 124



SN54S124 (J, W) SN74S124 (J, N)

NC—No internal connection

See page 7-123

†See explanation of function tables on page 3-8.

\*These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

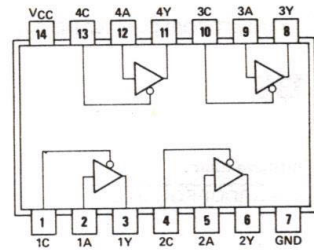
#### 125

positive logic:

$$Y = A$$

Output is off (disabled) when C is high.

See page 6-33



SN54125 (J, W) SN74125 (J, N)  
SN54LS125A (J, W) SN74LS125A (J, N)

### QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

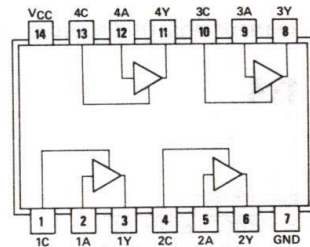
#### 126

positive logic:

$$Y = A$$

Output is off (disabled) when C is low.

See page 6-33



SN54126 (J, W) SN74126 (J, N)  
SN54LS126A (J, W) SN74LS126A (J, N)

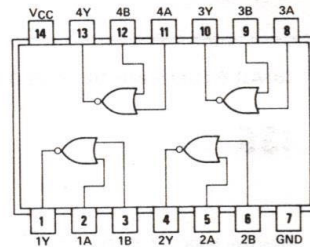
### SN54128 . . . 75-OHM LINE DRIVER SN74128 . . . 50-OHM LINE DRIVER

#### 128

positive logic:

$$Y = A+B$$

See page 6-22



SN54128 (J, W) SN74128 (J, N)

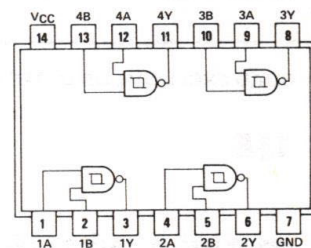
### QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

#### 132

positive logic:

$$Y = \overline{AB}$$

See page 6-14



SN54132 (J, W) SN74132 (J, N)  
SN54LS132 (J, W) SN74LS132 (J, N)  
SN54S132 (J, W) SN74S132 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

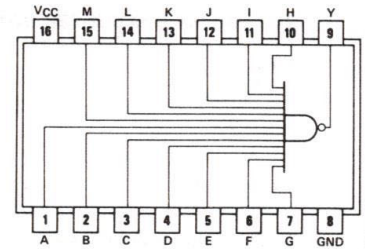
### 13-INPUT POSITIVE-NAND GATES

**133**

positive logic:

$$Y = \overline{ABCDEFGHIJKLM}$$

See page 6-2



SN54S133 (J, W) SN74S133 (J, N)

### 12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

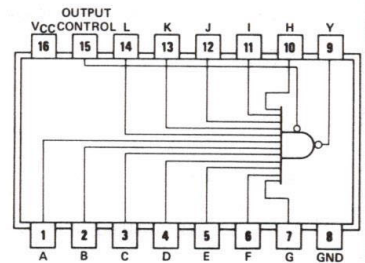
**134**

positive logic:

$$Y = \overline{ABCDEFGHIJKL}$$

Output is off (disabled) when output control is high.

See page 6-33



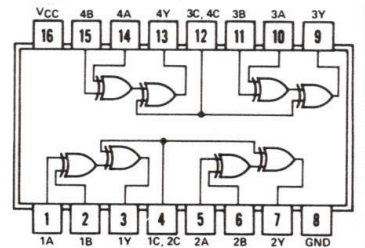
SN54S134 (J, W) SN74S134 (J, N)

### QUAD EXCLUSIVE-OR/NOR GATES

**135**

positive logic:  $Y = (A \oplus B) \oplus C = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$

See page 7-129



SN54S135 (J, W) SN74S135 (J, N)

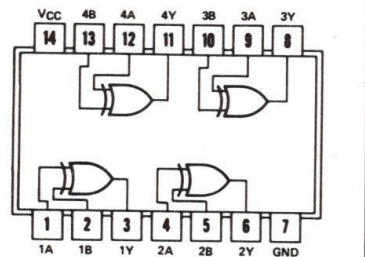
NC—No internal connection

### QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

**136**

positive logic:  $Y = A \oplus B = \overline{A}B + A\overline{B}$

See page 7-131



SN54136 (J, W) SN74136 (J, N)  
SN54LS136 (J, W) SN74LS136 (J, N)

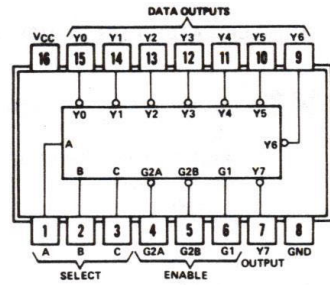
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEW)

### 3- TO 8-LINE DECODERS/DEMULTIPLEXERS

**138**

See page 7-134

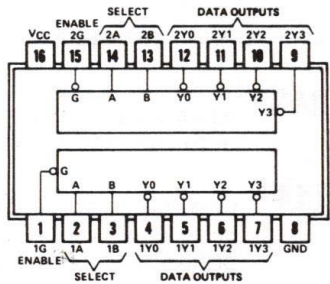


SN54LS138 (J, W) SN74LS138 (J, N)  
SN54S138 (J, W) SN74S138 (J, N)

### DUAL 2- TO 4-LINE DECODERS/DEMULTIPLEXERS

**139**

See page 7-134



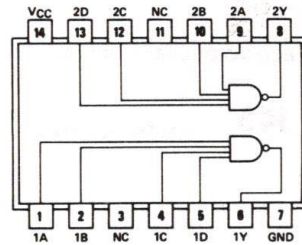
SN54LS139 (J, W) SN74LS139 (J, N)  
SN54S139 (J, W) SN74S139 (J, N)

### DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

**140**

positive logic:  
 $Y = ABCD$

See page 6-22



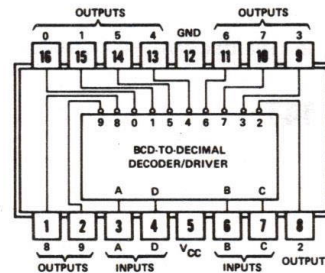
SN54S140 (J, W) SN74S140 (J, N)

NC—No internal connection

### BCD-TO-DECIMAL DECODER/DRIVER

**141** DRIVES COLD-CATHODE  
INDICATOR TUBES

See page 7-138



SN74141 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

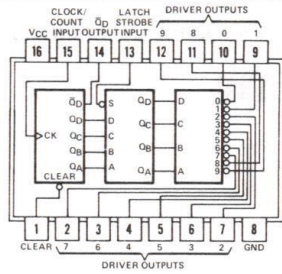
## PIN ASSIGNMENTS (TOP VIEWS)

### COUNTER/LATCH/DECODER/DRIVER

- 142** DIVIDE-BY-10 COUNTER  
4-BIT LATCH  
4-BIT TO 7-SEGMENT DECODER  
NIXIE ‡ TUBE DRIVER

See page 7-140

‡Nixie is a registered trademark of the Burroughs Corp.



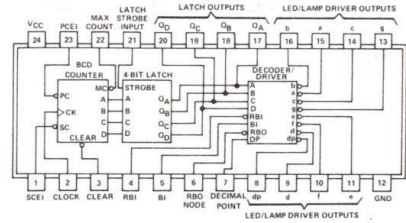
SN74142 (J, N)

### COUNTERS/LATCHES/DECODERS/DRIVERS

- 143** 15 mA CONSTANT CURRENT  
1- TO 5-V OUTPUT RANGE

- 144** UP TO 15-V INDICATORS  
UP TO 25 mA  
OPEN-COLLECTOR OUTPUT

See page 7-143

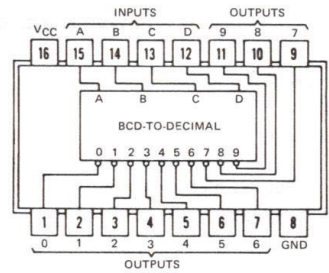


SN54143 (J, W) SN74143 (J, N)  
SN54144 (J, W) SN74144 (J, N)

### BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

- 145** BCD-TO-DECIMAL

See page 7-148

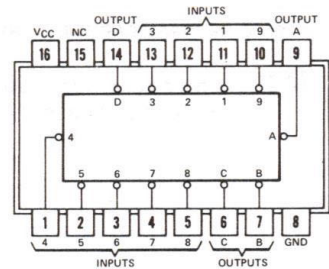


SN54145 (J, W) SN74145 (J, N)  
SN54LS145 (J, W) SN74LS145 (J, W)

### 10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

- 147**

See page 7-151



SN54147 (J, W) SN74147 (J, N)  
SN54LS147 (J, W) SN74LS147 (J, N)  
NC — No internal connection

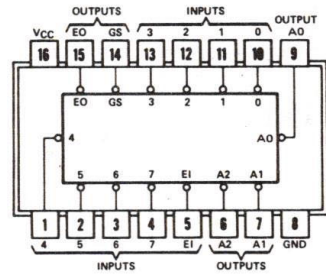
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

8-LINE-TO-3-LINE OCTAL PRIORITY ENCODERS

**148**

See page 7-151

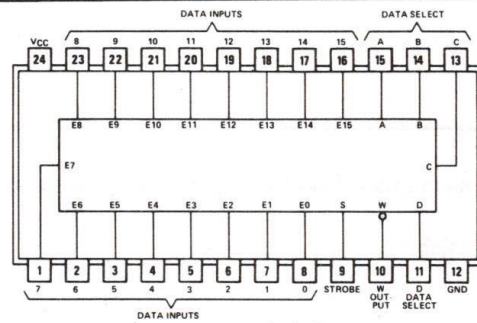


SN54148 (J, W) SN74148 (J, N)  
SN54LS148 (J, W) SN74LS148 (J, N)

1-OF-16 DATA SELECTORS/MULTIPLEXERS

**150**

See page 7-157

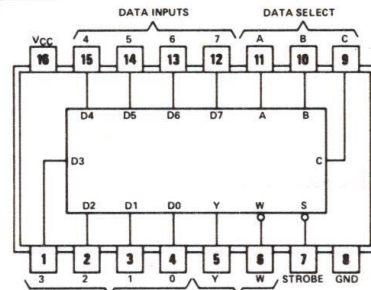


SN54150 (J, W) SN74150 (J, N)

1-OF-8 DATA SELECTORS/MULTIPLEXERS

**151**

See page 7-157

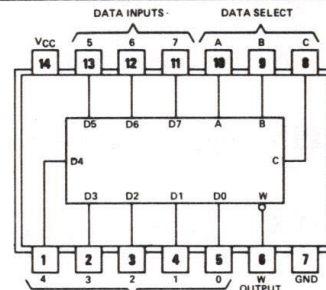


SN54151A (J, W) SN74151A (J, N)  
SN54LS151 (J, W) SN74LS151 (J, N)  
SN54S151 (J, W) SN74S151 (J, N)

1-OF-8 DATA SELECTORS/MULTIPLEXERS

**152**

See page 7-157



SN54152A (W)  
SN54LS152 (W)

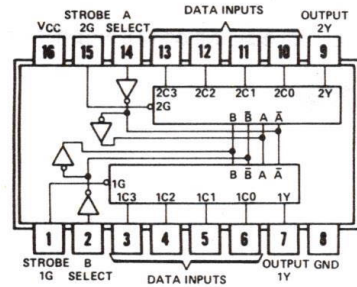


# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEW)

### DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

**153**

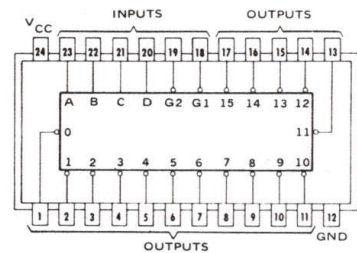


SN54153 (J, W)    SN74153 (J, N)  
 SN54L153 (J)    SN74L153 (J, N)  
 SN54LS153 (J, W)    SN74LS153 (J, N)  
 SN54S153 (J, W)    SN74S153 (J, N)

See page 7-165

### 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

**154**



SN54154 (J, W)    SN74154 (J, N)  
 SN54L154 (J)    SN74L154 (J, N)

See page 7-171

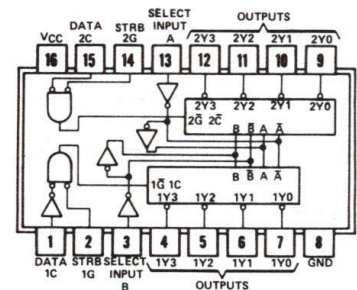
### DECODERS/DEMULTIPLEXERS

DUAL 2- TO 4-LINE DECODER  
 DUAL 1- TO 4-LINE DEMULTIPLEXER  
 3- TO 8-LINE DECODER  
 1- TO 8-LINE DEMULTIPLEXER

**155**    TOTEM-POLE OUTPUTS

**156**    OPEN-COLLECTOR OUTPUTS

See page 7-175



SN54155 (J, W)    SN74155 (J, N)  
 SN54LS155 (J, W)    SN74LS155 (J, N)  
 SN54156 (J, W)    SN74156 (J, N)  
 SN54LS156 (J, W)    SN74LS156 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

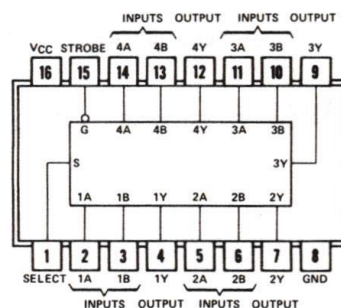
## PIN ASSIGNMENTS (TOP VIEW)

### QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

**157** NONINVERTED DATA OUTPUTS

**158** INVERTED DATA OUTPUTS

See page 7-181

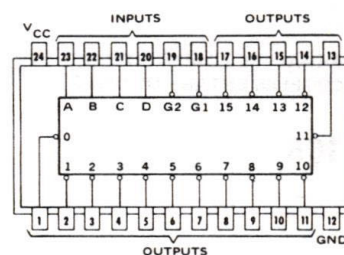


SN54157 (J, W)	SN74157 (J, N)
SN54L157 (J)	SN74L157 (J, N)
SN54LS157 (J, W)	SN74LS157 (J, N)
SN54S157 (J, W)	SN54S157 (J, N)
SN54LS158 (J, W)	SN74LS158 (J, N)
SN54S158 (J, W)	SN74S158 (J, N)

### 4- TO 16-LINE DECODERS/DEMULTIPLEXERS

**159** OPEN-COLLECTOR OUTPUTS

See page 7-188



SN54159 (J, W)	SN74159 (J, N)
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### SYNCHRONOUS 4-BIT COUNTERS

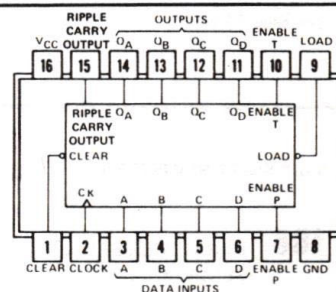
**160** DECADE, DIRECT CLEAR

**161** BINARY, DIRECT CLEAR

**162** DECADE, SYNCHRONOUS CLEAR

**163** BINARY, SYNCHRONOUS CLEAR

See page 7-190



SN54160 (J, W)	SN74160 (J, N)
SN54LS160A (J, W)	SN74LS160A (J, N)
SN54161 (J, W)	SN74161 (J, N)
SN54LS161A (J, W)	SN74LS161A (J, N)
SN54162 (J, W)	SN74162 (J, N)
SN54LS162A (J, W)	SN74LS162A (J, N)
SN54S162 (J, W)	SN74S162 (J, N)
SN54163 (J, W)	SN74163 (J, N)
SN54LS163A (J, W)	SN74LS163A (J, N)
SN54S163 (J, W)	SN74S163 (J, N)

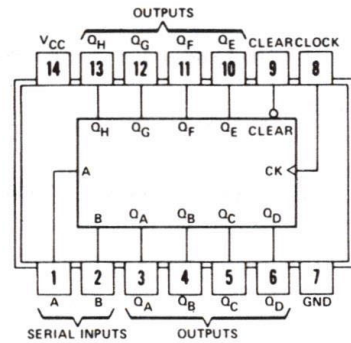
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS

#### 164 ASYNCHRONOUS CLEAR

See page 7-206

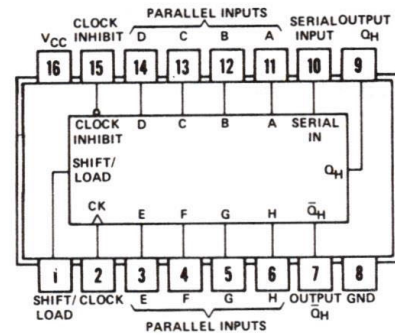


SN54164 (J, W)      SN74164 (J, N)  
 SN54L164 (J, T)    SN74L164 (J, N)  
 SN54LS164 (J, W)   SN74LS164 (J, N)

### PARALLEL-LOAD 8-BIT SHIFT REGISTERS WITH COMPLEMENTARY OUTPUTS

#### 165

See page 7-212

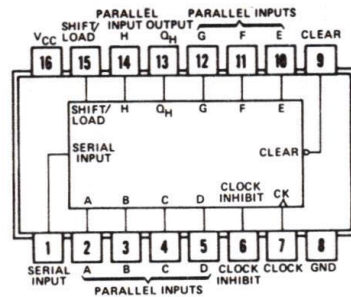


SN54165 (J, W)      SN74165 (J, N)  
 SN54LS165 (J, W)   SN74LS165 (J, N)

### 8-BIT SHIFT REGISTERS

#### 166 PARALLEL/SERIAL INPUT SERIAL OUTPUT

See page 7-217



SN54166 (J, W)      SN74166 (J, N)  
 SN54LS166 (J, W)   SN74LS166 (J, N)

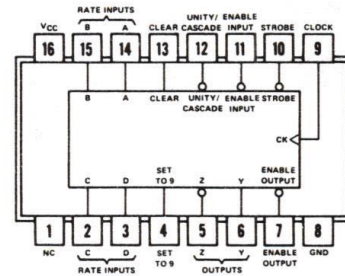
5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEW)

### SYNCHRONOUS DECADE RATE MULTIPLIERS

**167**



SN54167 (J, W)      SN74167 (J, N)

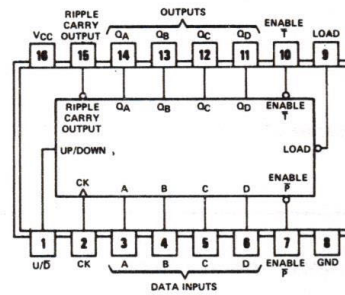
See page 7-222

NC — No internal connection

### 4-BIT UP/DOWN SYNCHRONOUS COUNTERS

**168**      DECADE

**169**      BINARY

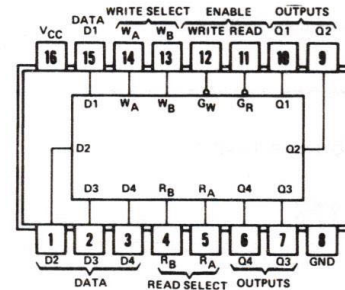


SN54S168 (J, W)      SN74S168 (J, N)  
 SN54LS169A (J, W)      SN74LS169A (J, N)  
 SN54S169 (J, W)      SN74S169 (J, N)

See page 7-226

### 4-BY-4 REGISTER FILES

**170**      SEPARATE READ/WRITE ADDRESSING  
 SIMULTANEOUS READ AND WRITE  
 OPEN-COLLECTOR OUTPUTS  
 EXPANDABLE TO 1024 WORDS



SN54170 (J, W)      SN74170 (J, N)  
 SN54LS170 (J, W)      SN74LS170 (J, N)

See page 7-237

5

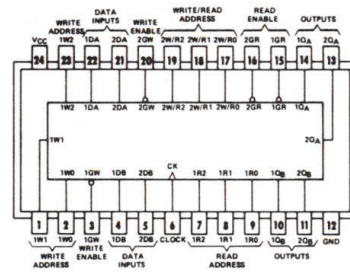
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 16-BIT REGISTER FILE

- 172** INDEPENDENT READ/WRITE ADDRESSING  
SIMULTANEOUS READ/WRITE  
8-WORDS OF TWO BITS EACH  
3-STATE OUTPUTS

See page 7-245

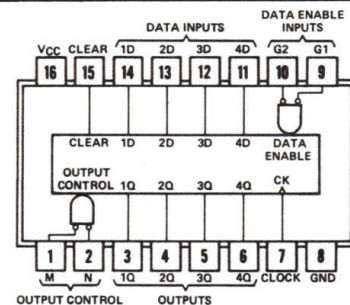


SN74172 (J, N)

### 4-BIT D-TYPE REGISTERS

- 173** 3-STATE OUTPUTS

See page 7-249

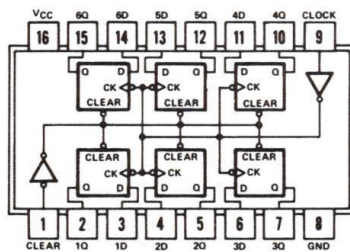


SN54173 (J, W) SN74173 (J, N)  
SN54LS173A (J, W) SN74LS173A (J, N)

### HEX D-TYPE FLIP-FLOPS

- 174** SINGLE-RAIL OUTPUTS  
COMMON DIRECT CLEAR

See page 7-253

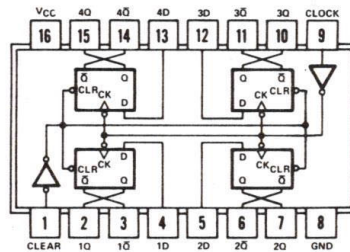


SN54174 (J, W) SN74174 (J, N)  
SN54LS174 (J, W) SN74LS174 (J, N)  
SN54S174 (J, W) SN74S174 (J, N)

### QUAD D-TYPE FLIP-FLOPS

- 175** COMPLEMENTARY OUTPUTS  
COMMON DIRECT CLEAR

See page 7-253



SN54175 (J, W) SN74175 (J, N)  
SN54LS175 (J, W) SN74LS175 (J, N)  
SN54S175 (J, W) SN74S175 (J, N)

5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

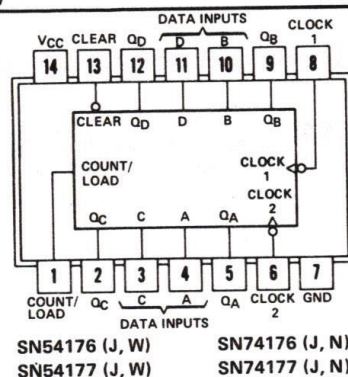
## PIN ASSIGNMENTS (TOP VIEWS)

### PRESETABLE COUNTERS/LATCHES

**176** DECADE (BI-QUINARY)

**177** BINARY

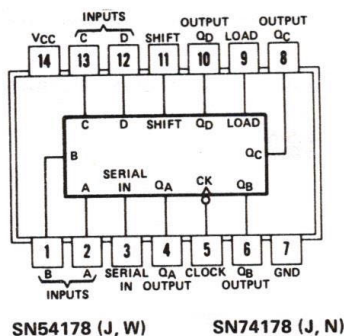
See page 7-259



### 4-BIT UNIVERSAL SHIFT REGISTERS

**178**

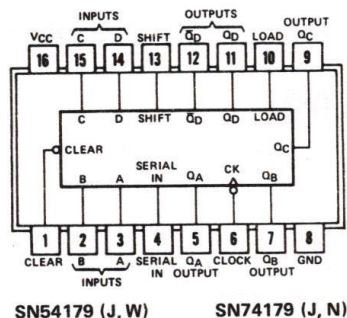
See page 7-265



### 4-BIT UNIVERSAL SHIFT REGISTERS

**179** DIRECT CLEAR  
Q<sub>D</sub> COMPLEMENTARY OUTPUTS

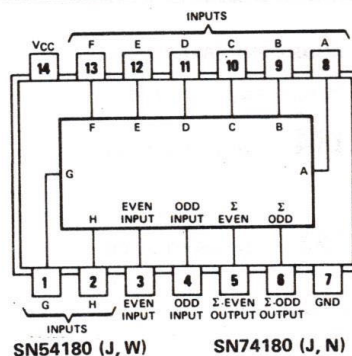
See page 7-265



### 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

**180**

See page 7-269



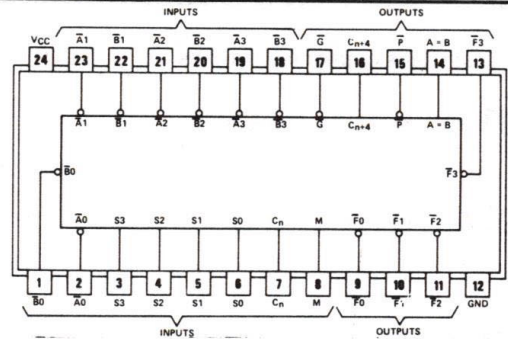
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

**181** 16 ARITHMETIC OPERATIONS  
16 LOGIC FUNCTIONS

See page 7-271

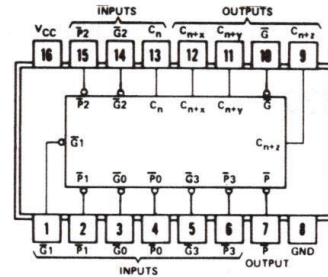


SN54181 (J, W) SN74181 (J, N)  
SN54LS181 (J, W) SN74LS181 (J, N)  
SN54S181 (J, W) SN74S181 (J, N)

### LOOK-AHEAD CARRY GENERATORS

**182**

See page 7-282

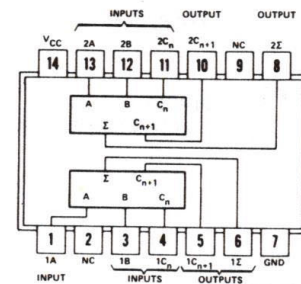


SN54182 (J, W) SN74182 (J, N)  
SN54S182 (J, W) SN74S182 (J, N)

### DUAL CARRY-SAVE FULL ADDERS

**183**

See page 7-287



SN54LS183 (J, W) SN74LS183 (J, N)  
SN54H183 (J, W) SN74H183 (J, N)

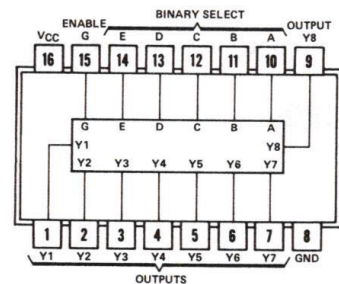
### CODE CONVERTERS

CASCADEABLE TO N-BITS

**184** BCD-TO-BINARY

**185** BINARY-TO-BCD

See page 7-290



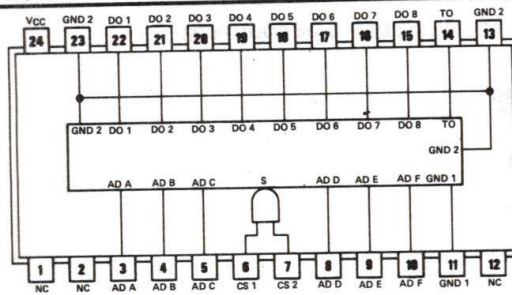
SN54184 (J, W) SN74184 (J, N)  
SN54185A (J, W) SN74185A (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 512-BIT PROGRAMMABLE READ-ONLY MEMORIES

**186** 64 8-BIT WORDS  
OPEN-COLLECTOR OUTPUTS

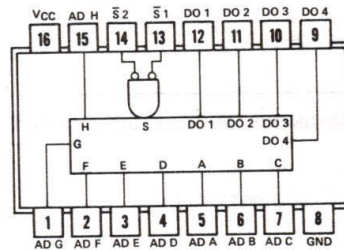


For more information contact the factory

SN54186 (J, W) SN74186 (J, N)  
NC - No internal connection

### 1024-BIT READ-ONLY MEMORIES

**187** 256 4-BIT WORDS  
OPEN-COLLECTOR OUTPUTS

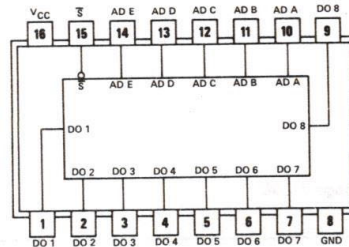


For more information contact the factory

SN54187 (J, W) SN74187 (J, N)

### 256-BIT PROGRAMMABLE READ-ONLY MEMORIES

**188** 32 8-BIT WORDS  
OPEN-COLLECTOR OUTPUTS

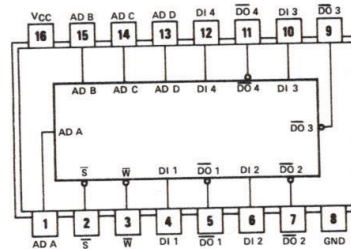


See Bipolar Microcomputer Components Data Book, second edition.

SN54S188 (J, W) SN74S188 (J, N)  
(Redesignated TBP18SA030)

### 64-BIT RANDOM-ACCESS MEMORIES

**189** 16 4-BIT WORDS  
THREE-STATE OUTPUTS



See Bipolar Microcomputer Components Data Book, second edition.

SN54S189 (J, W) SN74S189 (J, N)

5



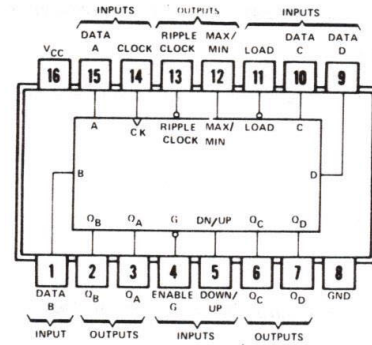
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### SYNCHRONOUS UP/DOWN COUNTERS

- 190** BCD
- 191** BINARY

See page 7-296

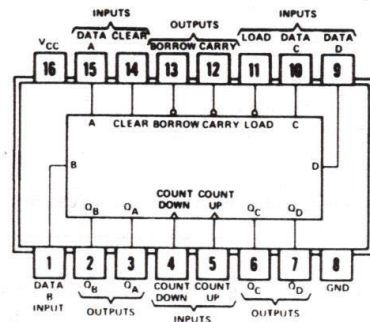


- SN54190 (J, W)
- SN54LS190 (J, W)
- SN54191 (J, W)
- SN54LS191 (J, W)
- SN74190 (J, N)
- SN74LS190 (J, N)
- SN74191 (J, N)
- SN74LS191 (J, N)

### SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

- 192** BCD WITH CLEAR
- 193** BINARY WITH CLEAR

See page 7-306

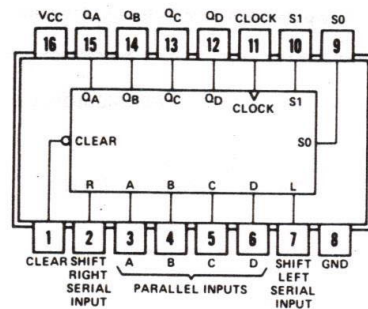


- SN54192 (J, W)
- SN54L192 (J)
- SN54LS192 (J, W)
- SN54193 (J, W)
- SN54L193 (J)
- SN54LS193 (J, W)
- SN74192 (J, N)
- SN74L192 (J, N)
- SN74LS192 (J, N)
- SN74193 (J, N)
- SN74L193 (J, N)
- SN74LS193 (J, N)

### 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- 194**

See page 7-316



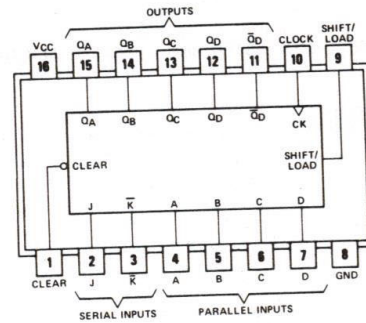
- SN54194 (J, W)
- SN54LS194A (J, W)
- SN54S194 (J, W)
- SN74194 (J, N)
- SN74LS194A (J, N)
- SN74S194 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

**195**



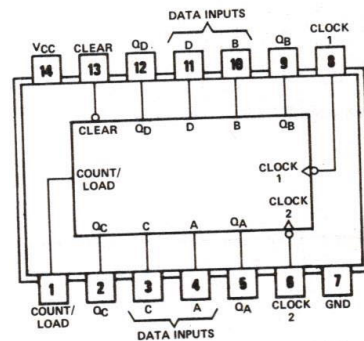
See page 7-324

SN54195 (J, W)      SN74195 (J, N)  
 SN54LS195A (J, W)      SN74LS195A (J, N)  
 SN54S195 (J, W)      SN74S195 (J, N)

### PRESETABLE COUNTERS/LATCHES

**196**    DECADE/BI-QUINARY

**197**    BINARY

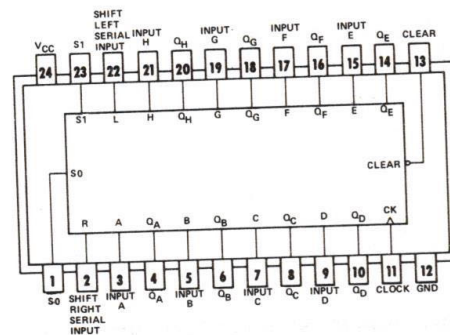


See page 7-331

SN54196 (J, W)      SN74196 (J, N)  
 SN54LS196 (J, W)      SN74LS196 (J, N)  
 SN54S196 (J, W)      SN74S196 (J, N)  
 SN54197 (J, W)      SN74197 (J, N)  
 SN54LS197 (J, W)      SN74LS197 (J, N)  
 SN54S197 (J, W)      SN74S197 (J, N)

### 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

**198**



See page 7-338

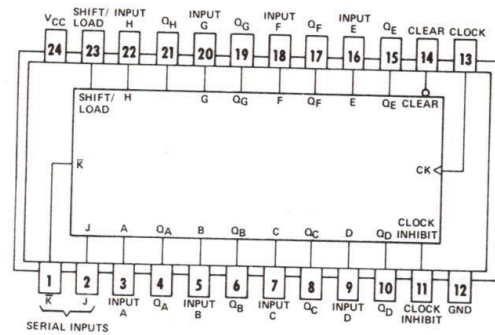
SN54198 (J, W)      SN74198 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

**199** J-K SERIAL INPUTS



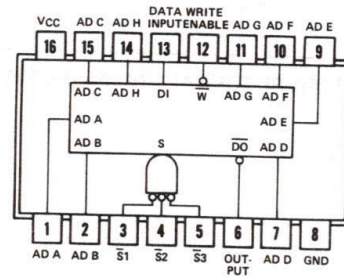
SN54199 (J, W) SN74199 (J, N)

See page 7-338

5

### 256-BIT RANDOM-ACCESS MEMORIES

**201** 256 1-BIT WORDS  
3-STATE OUTPUT



SN54S201 (J, W) SN74S201 (J, N)

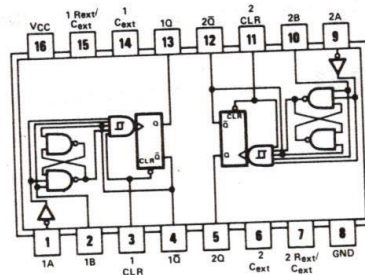
See Bipolar Microcomputer Components Data Book, second edition.

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL MONOSTABLE MULTIVIBRATORS

**221**

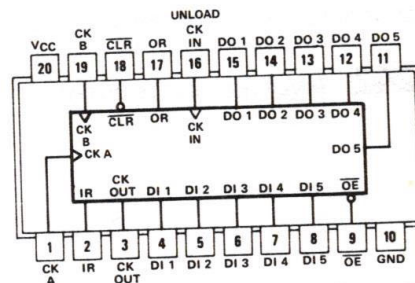


See page 6-68

SN54221 (J, W) SN74221 (J, N)  
SN54LS221 (J, W) SN74LS221 (J, N)

### ASYNCHRONOUS FIRST IN, FIRST OUT MEMORIES

**225** 16 5-BIT WORDS

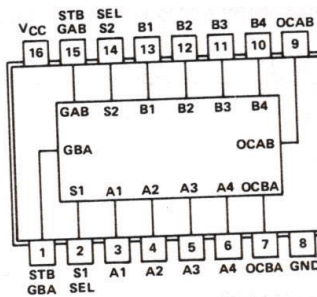


See Bipolar Microcomputer Components Data Book, second edition.

SN74S225 (J, N)

### 4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

**226** 3-STATE OUTPUTS

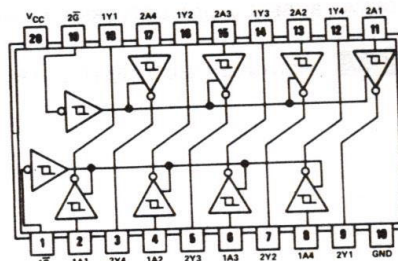


See page 7-345

SN54S226 (J, W) SN74S226 (J, N)

### OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

**240** INVERTED 3-STATE OUTPUTS



See page 6-83

SN54LS240 (J) SN74LS240 (J, N)  
SN54S240 (J) SN74S240 (J, N)

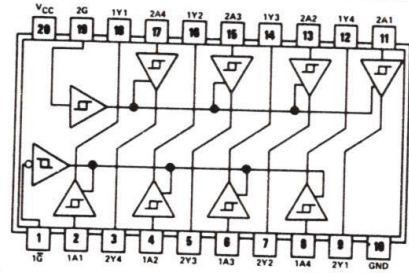
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

**241** NONINVERTED 3-STATE OUTPUTS

See page 6-83

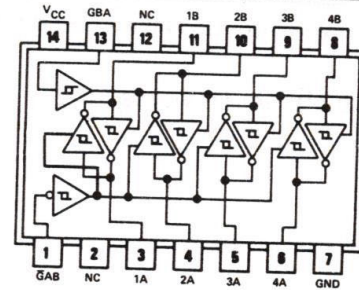


SN54LS241 (J) SN74LS241 (J, N)  
SN54S241 (J) SN74S241 (J, N)

QUADRUPLE BUS TRANSCEIVERS

**242** INVERTED 3-STATE OUTPUTS

See page 6-87

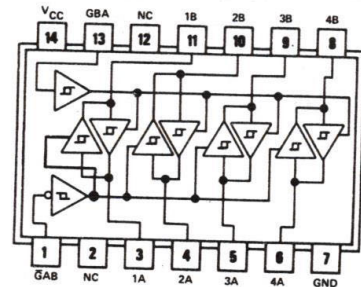


SN54LS242 (J, W) SN74LS242 (J, N)  
NC—No internal connection

QUADRUPLE BUS TRANSCEIVERS

**243** NONINVERTED 3-STATE OUTPUTS

See page 6-87

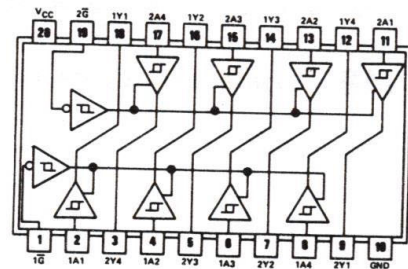


SN54LS243 (J, W) SN74LS243 (J, N)  
NC—No internal connection

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

**244** NONINVERTED 3-STATE OUTPUTS

See page 6-83



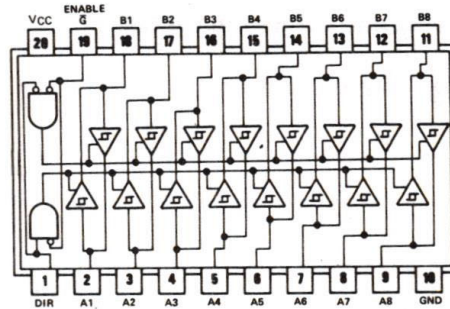
SN54LS244 (J) SN74LS244 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### OCTAL BUS TRANCEIVERS

**245** NONINVERTED 3-STATE OUTPUTS



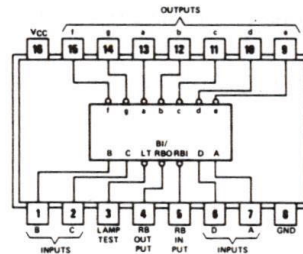
SN54LS245 (J) SN74LS245 (J, N)

See page 7-349

### BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**246** ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

**247** ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS



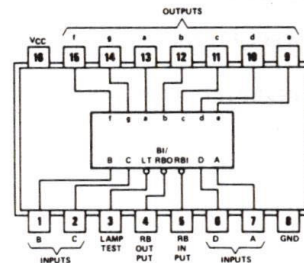
SN54246 (J, W) SN74246 (J, N)  
SN54247 (J, W) SN74247 (J, N)  
SN54LS247 (J, W) SN74LS247 (J, N)

See page 7-351

### BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

**248** INTERNAL PULL-UP OUTPUTS

**249** OPEN-COLLECTOR OUTPUTS

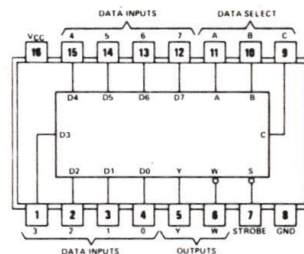


SN54248 (J, W) SN74248 (J, N)  
SN54LS248 (J, W) SN74LS248 (J, N)  
SN54249 (J, W) SN74249 (J, N)  
SN54LS249 (J, W) SN74LS249 (J, N)

See page 7-351

### DATA SELECTORS/MULTIPLEXERS

**251** TRUE AND INVERTED 3-STATE OUTPUTS



SN54251 (J, W) SN74251 (J, N)  
SN54LS251 (J, W) SN74LS251 (J, N)  
SN54S251 (J, W) SN74S251 (J, N)

See page 7-362

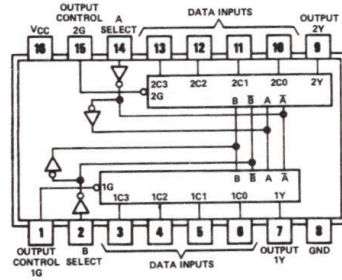
5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL DATA SELECTORS/MULTIPLEXERS

**253** 3-STATE OUTPUTS

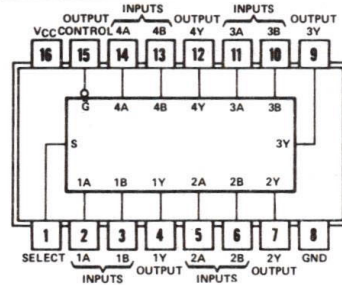


See page 7-369

SN54LS253 (J, W) SN74LS253 (J, N)

### QUAD DATA SELECTORS/MULTIPLEXERS

**257** NONINVERTED 3-STATE OUTPUTS

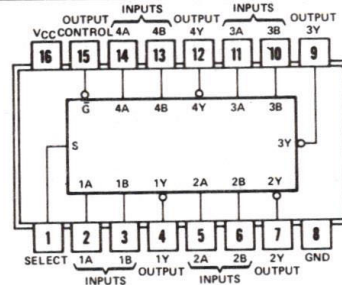


See page 7-372

SN54LS257A (J, W) SN74LS257A (J, N)  
SN54S257 (J, W) SN74S257 (J, N)

### QUAD DATA SELECTORS/MULTIPLEXERS

**258** INVERTED 3-STATE OUTPUTS

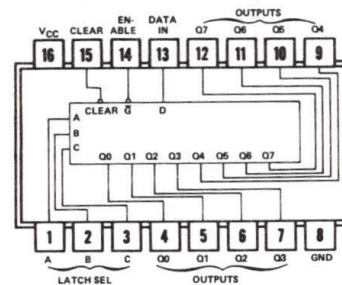


See page 7-372

SN54LS258A (J, W) SN74LS258A (J, N)  
SN54S258 (J, W) SN74S258 (J, N)

### EIGHT-BIT ADDRESSABLE LATCHES

**259**



See page 7-376

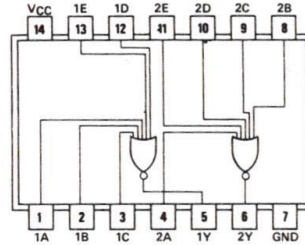
SN54259 (J, W) SN74259 (J, N)  
SN54LS259 (J, W) SN74LS259 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

DUAL 5-INPUT POSITIVE NOR GATES

**260**

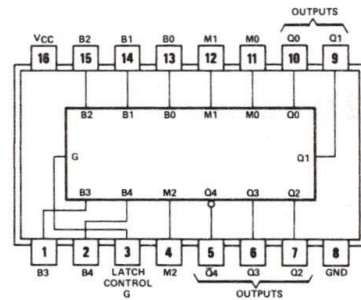


See page 6-8

SN54S260 (J, W) SN74S260 (J, N)

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

**261**

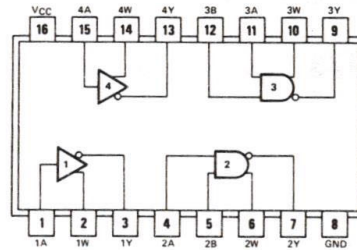


See page 7-380

SN54LS261 (J, W) SN74LS261 (J, N)

QUAD COMPLEMENTARY-OUTPUT ELEMENTS

**265**



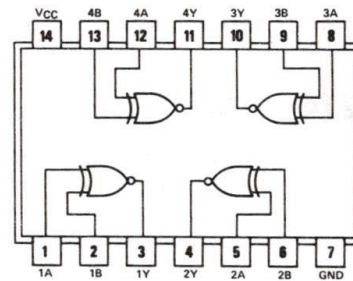
See page 6-89

SN54265 (J, W) SN74265 (J, N)

QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

**266**

positive logic:  $Y = A \oplus B = AB + \overline{AB}$



See page 7-386

SN54LS266 (J, W) SN74LS266 (J, N)

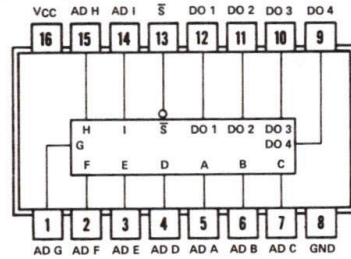


# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 2048-BIT READ-ONLY MEMORIES

**270** OPEN-COLLECTOR OUTPUTS  
512 4-BIT WORDS

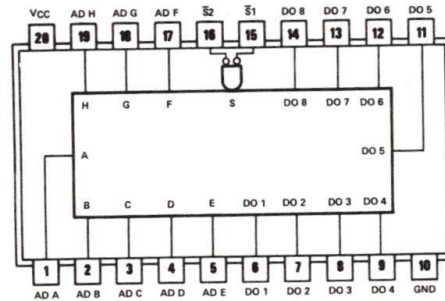


For more information contact the factory

SN54S270 (J) SN74S270 (J, N)

### 2048-BIT READ-ONLY MEMORIES

**271** OPEN-COLLECTOR OUTPUTS  
256 8-BIT WORDS

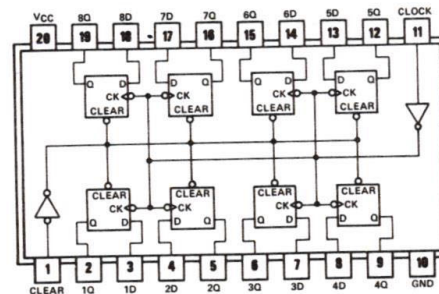


For more information contact the factory

SN54S271 (J) SN74S271 (J, N)

### OCTAL D-TYPE FLIP-FLOPS

**273** COMMON CLOCK  
SINGLE-RAIL OUTPUTS

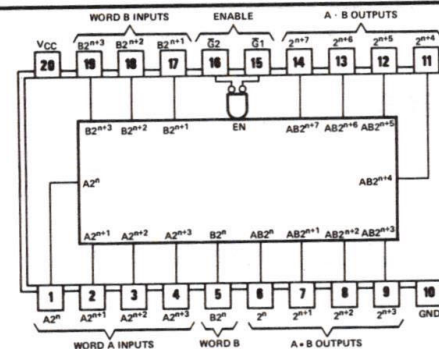


See page 7-388

SN54273 (J) SN74273 (J, N)  
SN54LS273 (J) SN74LS273 (J, N)

### 4-BIT BY 4-BIT BINARY MULTIPLIERS

**274** 3-STATE OUTPUTS  
8-BIT PRODUCTS  
SUB-MULTIPLE PRODUCTS



See page 7-391

SN54S274 (J) SN74S274 (J, N)

5

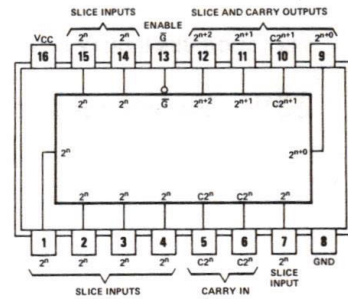
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEW)

### 7-BIT SLICE WALLACE TREES

**275** 3-STATE OUTPUTS

See page 7-391

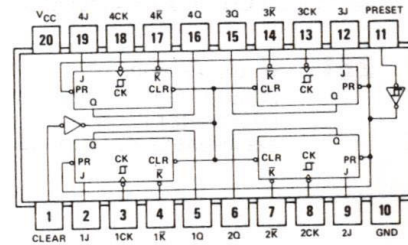


SN54LS275 (J) SN74LS275 (J, N)  
SN54S275 (J) SN74S275 (J, N)

### QUAD J-K̄ FLIP-FLOPS

**276** SEPARATE CLOCKS  
EDGE-TRIGGERING  
COMMON DIRECT CLEAR AND PRESET

See page 7-401

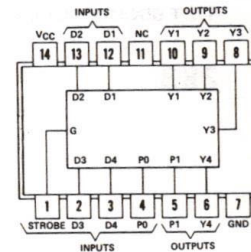


SN54276 (J) SN74276 (J, N)

### 4-BIT CASCADEABLE PRIORITY REGISTERS

**278** LATCHED DATA INPUTS  
PRIORITY OUTPUT GATING

See page 7-403



SN54278 (J, W) SN74278 (J, N)  
NC — No internal connection

### QUAD S̄-R̄ LATCHES

**279** DIODE-CLAMPED INPUTS  
TOTEM-POLE OUTPUTS

H = high level  
L = low level

Q<sub>0</sub> = the level of Q before the indicated input conditions were established.

\* This output level is pseudo stable; that is, it may not persist when the S̄ and R̄ inputs return to their inactive (high) level.

† For latches with double S̄ inputs:

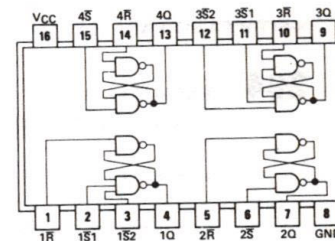
H = both S̄ inputs high

L = one or both S̄ inputs low

See page 6-60

#### FUNCTION TABLE

INPUTS		OUTPUT
S̄†	R̄	Q
H	H	Q <sub>0</sub>
L	H	H
H	L	L
L	L	H*



SN54279 (J, W) SN74279 (J, N)  
SN54LS279 (J, W) SN74LS279 (J, N)

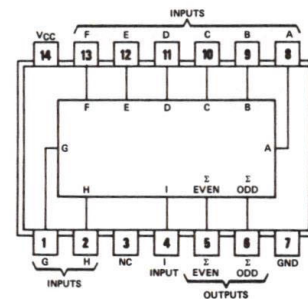
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

**280** N-BIT CASCADEABLE

See page 7-406

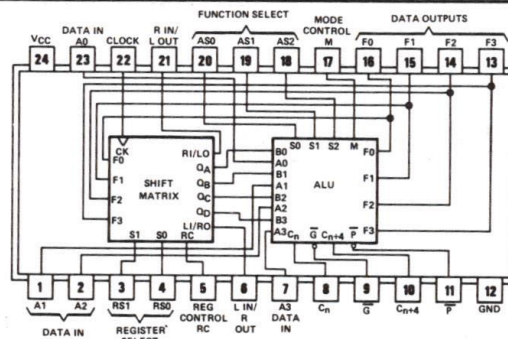


SN54LS280 (J, W) SN74LS280 (J, N)  
SN54S280 (J, W) SN74S280 (J, N)

### 4-BIT PARALLEL BINARY ACCUMULATORS

**281** 15 ARITHMETIC/  
LOGIC-TYPE OPERATIONS  
LOGIC SHIFT (L OR R)  
EXPANDABLE TO N WORDS

See page 7-410

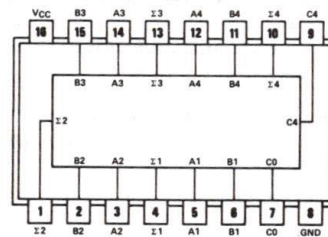


SN54S281 (J, W) SN74S281 (J, N)

### 4-BIT BINARY FULL ADDERS

**283**

See page 7-415



SN54283 (J, W) SN74283 (J, N)  
SN54LS283 (J, W) SN74LS283 (J, N)  
SN54S283 (J) SN74S283 (J, N)

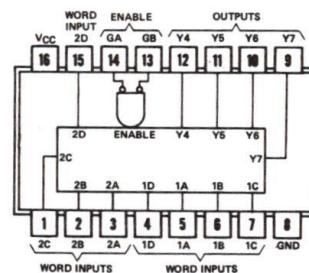
### 4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '285

**284** EXPANDABLE FOR N-BIT-  
BY-N-BIT MULTIPLICATION

USE 'S274 FOR NEW DESIGNS

USE 'LS275/'S275 FOR LARGE MULTIPLIERS

See page 7-420



SN54284 (J, W) SN74284 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

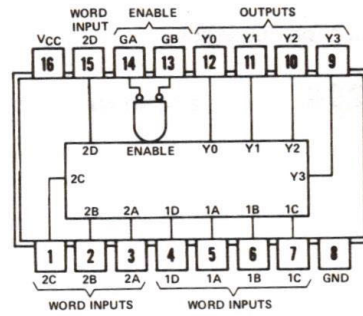
### 4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '284

**285** EXPANDABLE FOR N-BIT-BY-N-BIT MULTIPLICATION

USE 'S274 FOR NEW DESIGNS

USE 'LS275/'S275 FOR LARGE MULTIPLIERS

See page 7-420

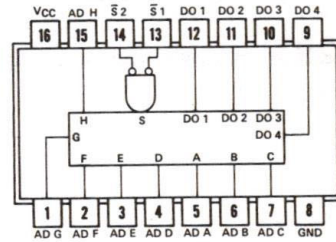


SN54285 (J, W) SN74285 (J, N)

### 1024-BIT PROGRAMMABLE READ-ONLY MEMORIES

**287** 256 4-BIT WORDS  
3-STATE OUTPUTS

See Bipolar Microcomputer Components Data Book, second edition.

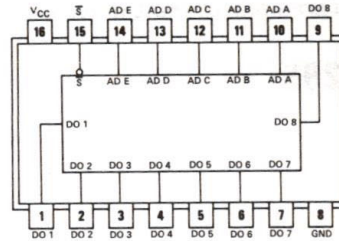


SN54S287 (J, W) SN74S287 (J, N)  
(Redesignated TBP14S10)

### 256-BIT PROGRAMMABLE READ-ONLY MEMORIES

**288** 32 8-BIT WORDS  
3-STATE OUTPUTS

See Bipolar Microcomputer Components Data Book, second edition.

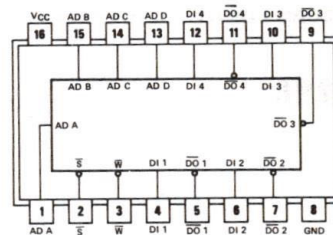


SN54288 (J, W) SN74S288 (J, N)  
(Redesignated TBP18S030)

### 64-BIT RANDOM-ACCESS MEMORIES

**289** 16 4-BIT WORDS  
OPEN-COLLECTOR OUTPUTS

See Bipolar Microcomputer Components Data Book, second edition.



SN54S289 (J, W) SN74S289 (J, N)

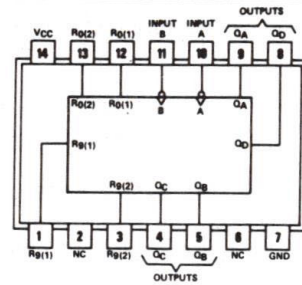
5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DECADE COUNTERS

**290** DIVIDE-BY-TWO AND DIVIDE-BY-5

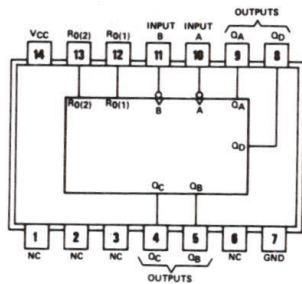


See page 7-423

SN54290 (J, W) SN74290 (J, N)  
SN54LS290 (J, W) SN74LS290 (J, N)

### 4-BIT BINARY COUNTERS

**293** DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT

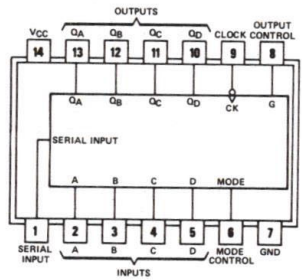


See page 7-423

SN54293 (J, W) SN74293 (J, N)  
SN54LS293 (J, W) SN74LS293 (J, N)

### 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

**295**

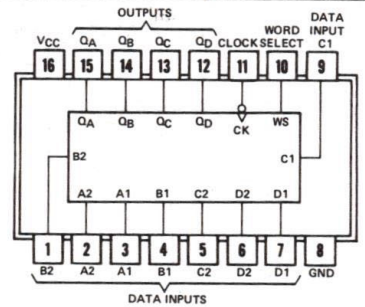


See page 7-429

SN54LS295B (J, W) SN74LS295B (J, N)

### QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

**298**



See page 7-432

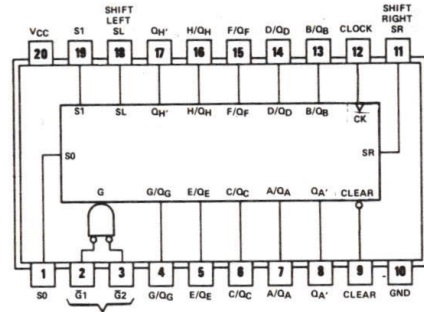
SN54298 (J, W) SN74298 (J, N)  
SN54LS298 (J, W) SN74LS298 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

**299** 3-STATE OUTPUTS



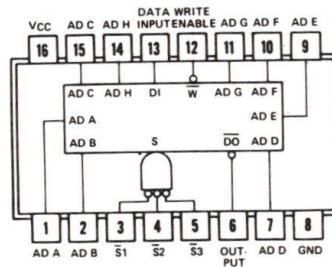
SN54LS299 (J)  
SN54S299 (J)

SN74LS299 (J, N)  
SN74S299 (J, N)

See page 7-437

### 256-BIT RANDOM ACCESS MEMORIES

**301** 256 1-BIT WORDS  
OPEN-COLLECTOR OUTPUT

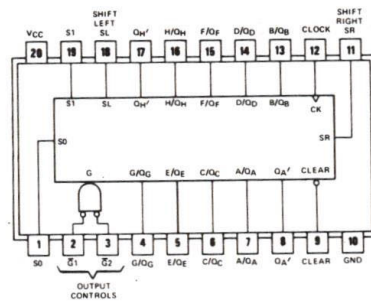


SN54S301 (J, W) SN74S301 (J, N)

See Bipolar Microcomputer Components Data Book, second edition.

### 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

**323** 3-STATE OUTPUTS



SN54LS323 (J)

SN74LS323 (J, N)

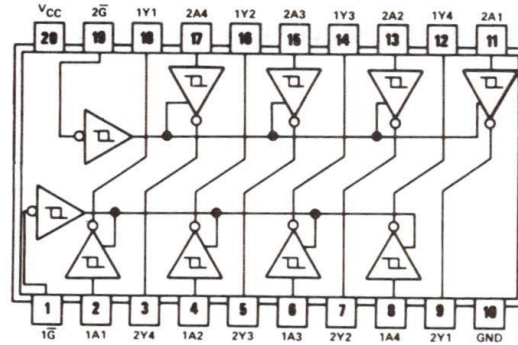
See page 7-443

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUFFERS/LINE DRIVERS

**340** 3-STATE INVERTED OUTPUTS

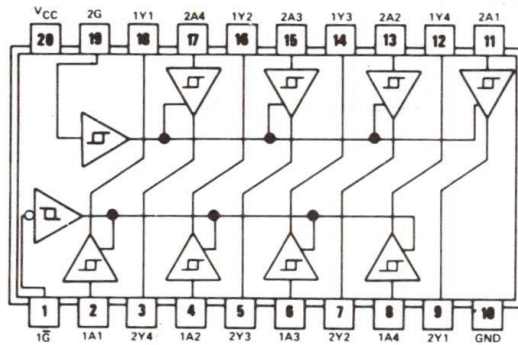


See page 7-445

SN74S340 (J, N)

OCTAL BUFFERS/LINE DRIVERS

**341** 3-STATE NONINVERTED OUTPUTS

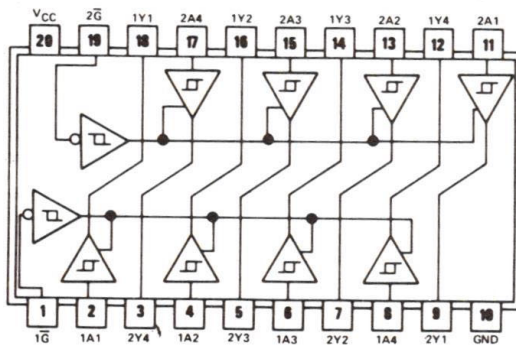


See page 7-445

SN74S341 (J, N)

OCTAL BUFFERS/LINE DRIVERS

**344** 3-STATE NONINVERTED OUTPUTS



See page 7-445

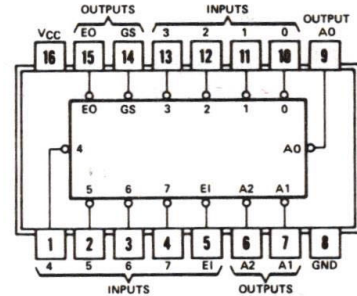
SN74S344 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 8-LINE TO 3-LINE PRIORITY ENCODERS

**348** 3-STATE OUTPUTS

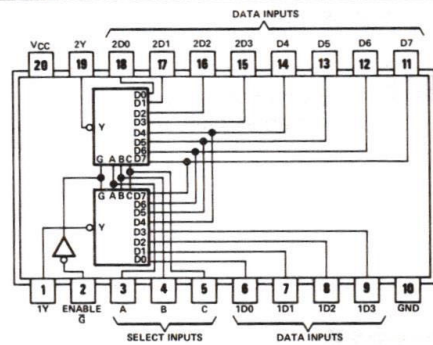


See page 7-448

SN54LS348 (J, W) SN74LS348 (J, N)

### DUAL 8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

**351** 3-STATE OUTPUTS  
4 COMMON DATA INPUTS

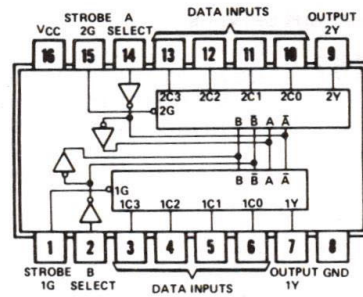


See page 7-451

SN74351 (N)

### DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

**352** INVERTING VERSION OF 'LS153

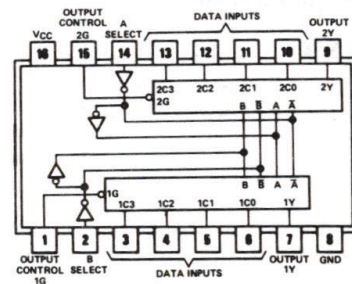


See page 7-454

SN54LS352 (J, W) SN74LS352 (J, N)

### DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

**353** 3-STATE OUTPUTS  
INVERTING VERSION OF 'LS253



See page 7-457

SN54LS353 (J, W) SN74LS353 (J, N)

5



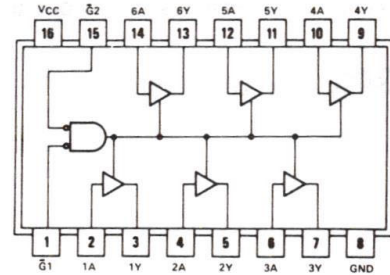
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### HEX BUS DRIVERS

**365** NONINVERTED 3-STATE OUTPUTS  
GATED ENABLE INPUTS

See page 6-36

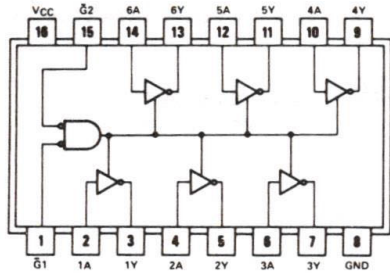


SN54365A (J, W) SN74365A (J, N)  
SN54LS365A (J, W) SN74LS365A (J, N)

### HEX BUS DRIVERS

**366** INVERTED 3-STATE OUTPUTS  
GATED ENABLE INPUTS

See page 6-36

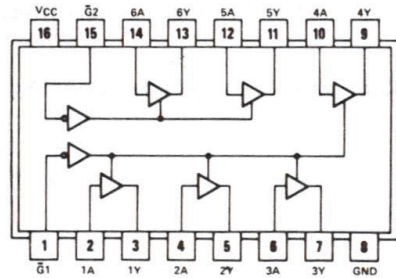


SN54366A (J, W) SN74366A (J, N)  
SN54LS366A (J, W) SN74LS366A (J, N)

### HEX BUS DRIVERS

**367** NONINVERTED 3-STATE OUTPUTS  
ORGANIZED TO FACILITATE  
HANDLING OF 4-BIT DATA

See page 6-36

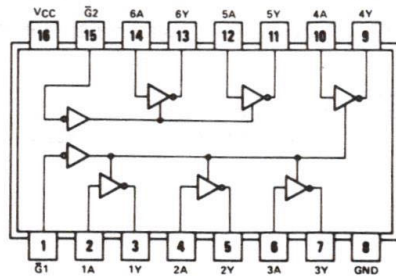


SN54367A (J, W) SN74367A (J, N)  
SN54LS367A (J, W) SN74LS367A (J, N)

### HEX BUS DRIVERS

**368** INVERTED 3-STATE OUTPUTS  
ORGANIZED TO FACILITATE  
HANDLING OF 4-BIT DATA

See page 6-36



SN54368A (J, W) SN74368A (J, N)  
SN54LS368A (J, W) SN74LS368A (J, N)

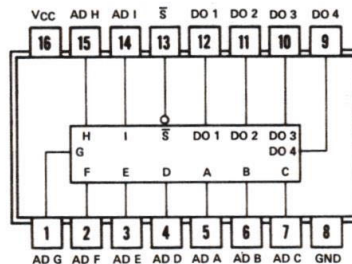
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 2048-BIT READ-ONLY MEMORIES

**370**

512 4-BIT WORDS  
3-STATE OUTPUTS



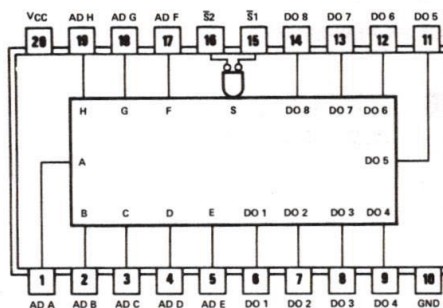
For more information contact the factory

SN54S370 (J) SN74S370 (J, N)

### 2048-BIT READ-ONLY MEMORIES

**371**

256 8-BIT WORDS  
3-STATE OUTPUTS



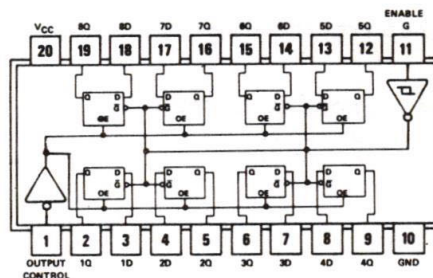
For more information contact the factory

SN54S371 (J) SN74S371 (J, N)

### OCTAL D-TYPE LATCHES

**373**

3-STATE OUTPUTS  
COMMON OUTPUT CONTROL  
COMMON ENABLE



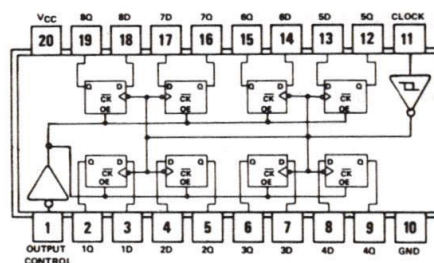
See page 7-471

SN54LS373 (J) SN74LS373 (J, N)  
SN54S373 (J) SN74S373 (J, N)

### OCTAL D-TYPE FLIP-FLOPS

**374**

3-STATE OUTPUTS  
COMMON OUTPUT CONTROL  
COMMON CLOCK



See page 7-471

SN54LS374 (J) SN74LS374 (J, N)  
SN54S374 (J) SN74S374 (J, N)

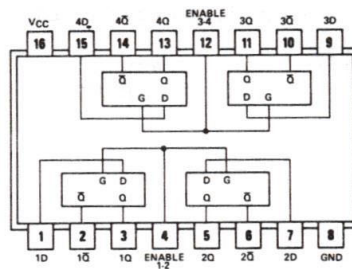
5

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

4-BIT BISTABLE LATCHES

**375**



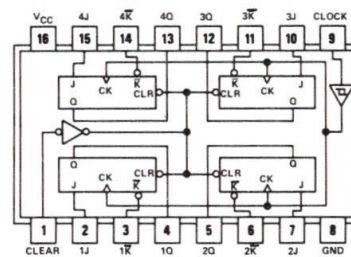
See page 7-478

SN54LS375 (J, W) SN74LS375 (J, N)

QUAD J-K̄ FLIP-FLOPS

**376**

COMMON CLOCK  
COMMON CLEAR



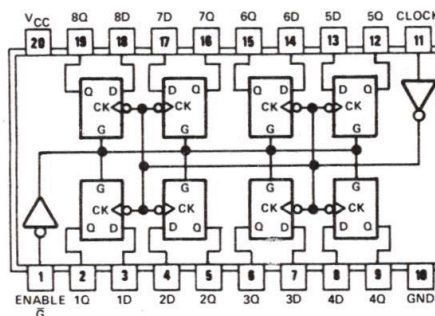
See page 7-479

SN54376 (J, W) SN74376 (J, N)

OCTAL D-TYPE FLIP-FLOPS

**377**

SINGLE-RAIL OUTPUTS  
COMMON ENABLE  
COMMON CLOCK



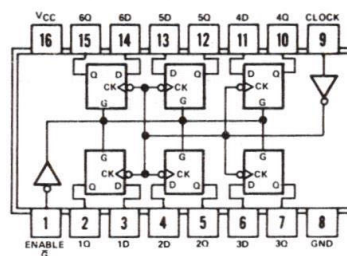
See page 7-481

SN54LS377 (J) SN74LS377 (J, N)

HEX D-TYPE FLIP-FLOPS

**378**

SINGLE-RAIL OUTPUTS  
COMMON ENABLE  
COMMON CLOCK



See page 7-481

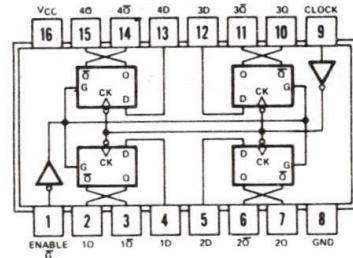
SN54LS378 (J, W) SN74LS378 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### QUAD D-TYPE FLIP-FLOPS

**379** DOUBLE-RAIL OUTPUTS  
COMMON ENABLE  
COMMON CLOCK

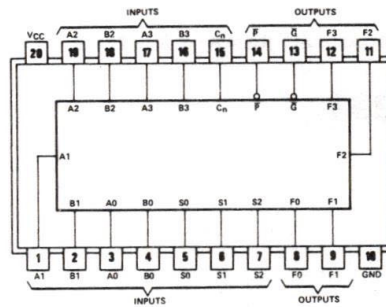


See page 7-481

SN54LS379 (J, W) SN74LS379 (J, N)

### ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

**381** 8 BINARY FUNCTIONS  
USE 'S182 FOR LOOK-AHEAD CARRY

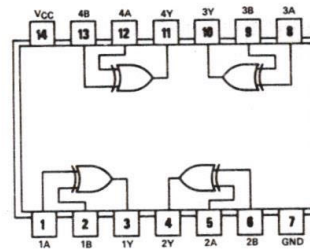


See page 7-484

SN54S381 (J) SN74S381 (J, N)

### QUAD 2-INPUT EXCLUSIVE-OR GATES

**386**  
POSITIVE LOGIC:  
 $Y = A \oplus B = \bar{A}B + A\bar{B}$

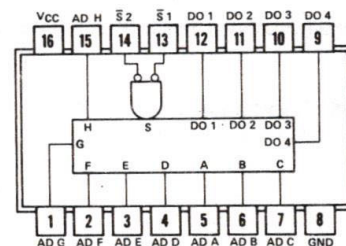


See page 7-487

SN54LS386 (J, W) SN74LS386 (J, N)

### 1024-BIT PROGRAMMABLE READ-ONLY MEMORIES

**387** 256 4-BIT WORDS  
OPEN-COLLECTOR OUTPUTS



See Bipolar Microcomputer Components Data Book, second edition.

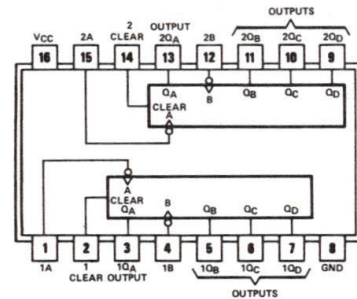
SN54S387 (J, W) SN74S387 (J, N)  
(Redesignated TBP14SA10)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL DECADE COUNTERS

**390** BI-QUINARY OR BCD SEQUENCES

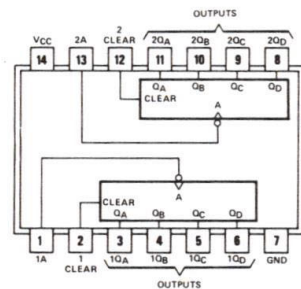


See page 7-489

SN54390 (J, W) SN74390 (J, N)  
SN54LS390 (J, W) SN74LS390 (J, N)

### DUAL 4-BIT BINARY COUNTERS

**393**

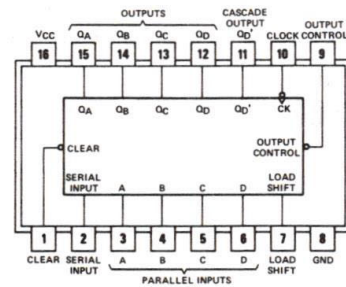


See page 7-489

SN54393 (J, W) SN74393 (J, N)  
SN54LS393 (J, W) SN74LS393 (J, N)

### 4-BIT UNIVERSAL SHIFT REGISTERS

**395** 3-STATE OUTPUTS

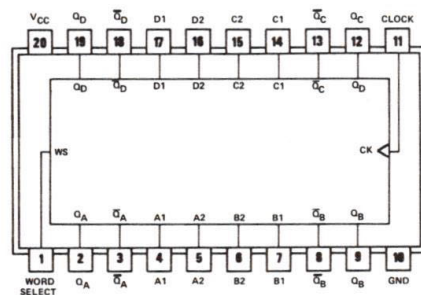


See page 7-496

SN54LS395A (J, W) SN74LS395A (J, N)

### QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

**398** DOUBLE-RAIL OUTPUTS



See page 7-499

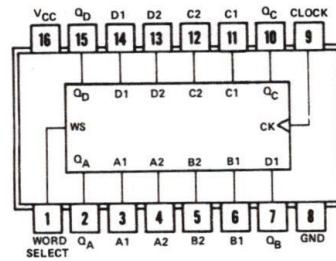
SN54LS398 (J) SN74LS398 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

**399** SINGLE-RAIL OUTPUTS

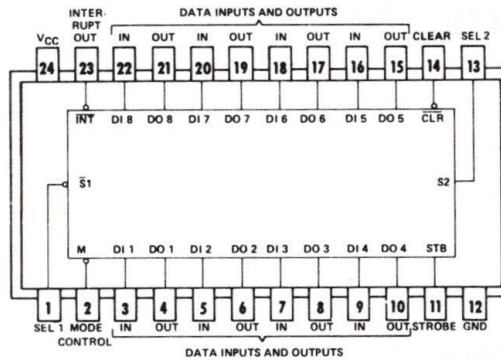


See page 7-499

SN54LS399 (J,W) SN74LS399 (J, N)

### MULTI-MODE BUFFERED 8-BIT LATCHES

**412** 3-STATE OUTPUTS  
DIRECT CLEAR



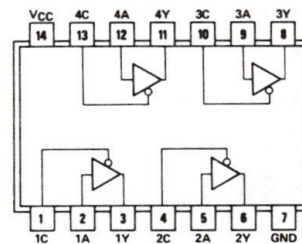
See page 7-502

SN54S412 (J) SN74S412 (J, N)

### QUAD GATES

**425** 3-STATE OUTPUTS  
ACTIVE-LOW ENABLING

positive logic:  $Y = A$



See page 6-33

SN54425 (J, W) SN74425 (J, N)

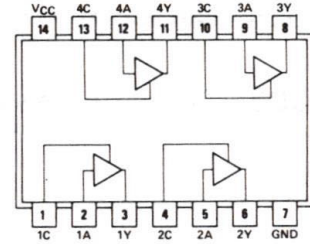
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### QUAD GATES

**426** 3-STATE OUTPUTS  
ACTIVE-HIGH ENABLING

positive logic:  $Y = A$



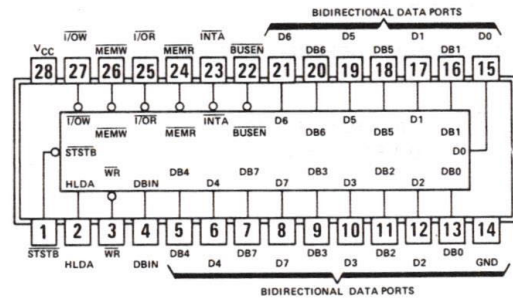
See page 6-33

SN54426 (J, W) SN74426 (J, N)

### SYSTEM CONTROLLER FOR 8080A

**428** BIDIRECTIONAL DATA PORTS

**438** BIDIRECTIONAL DATA PORTS



See page 7-514

SN74S428 (N)  
SN74S438 (N)

### QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

**440** OPEN-COLLECTOR NONINVERTED OUTPUTS

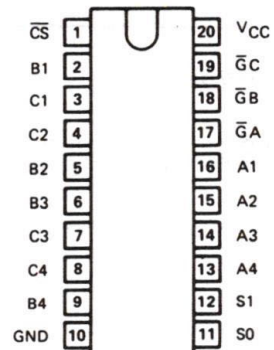
**441** OPEN-COLLECTOR INVERTED OUTPUTS

**442** 3-STATE NONINVERTED OUTPUTS

**443** 3-STATE INVERTED OUTPUTS

**444** 3-STATE INVERTED AND NONINVERTED OUTPUTS

**448** OPEN-COLLECTOR INVERTED AND NONINVERTED OUTPUTS



See page 7-507

SN54LS440 (J) SN74LS440 (J, N)  
SN54LS441 (J) SN74LS441 (J, N)  
SN54LS442 (J) SN74LS442 (J, N)  
SN54LS443 (J) SN74LS443 (J, N)  
SN54LS444 (J) SN74LS444 (J, N)  
SN54LS448 (J) SN74LS448 (J, N)

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

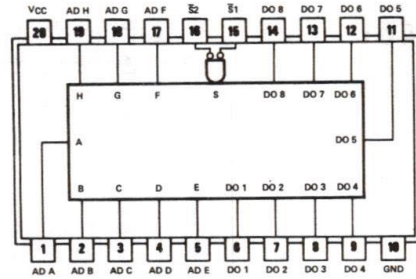
## PIN ASSIGNMENTS (TOP VIEWS)

### PROGRAMMABLE READ-ONLY MEMORIES

256 8-BIT WORDS

**470** OPEN-COLLECTOR OUTPUTS

**471** 3-STATE OUTPUTS



SN54S470 (J) SN74S470 (J, N)  
(Redesignated TBP18SA22)

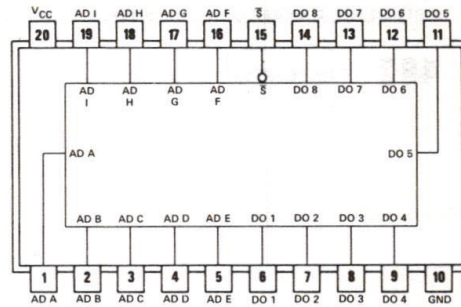
SN54S471 (J) SN74S471 (J, N)  
(Redesignated TBP18S22)

See Bipolar Microcomputer Components Data Book, second edition.

### PROGRAMMABLE READ-ONLY MEMORIES

**472** 3-STATE OUTPUTS

**473** OPEN-COLLECTOR OUTPUTS



SN54S472 (J) SN74S472 (J, N)  
(Redesignated TBP18S42)

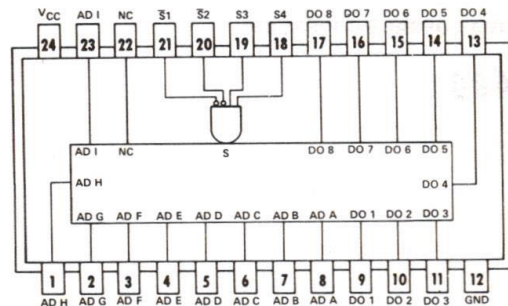
SN54S473 (J) SN74S473 (J, N)  
(Redesignated TBP18SA42)

See Bipolar Microcomputer Components Data Book, second edition.

### PROGRAMMABLE READ-ONLY MEMORIES

**474** 3-STATE OUTPUTS

**475** OPEN-COLLECTOR OUTPUTS



SN54S474 (J) SN74S474 (J, N)  
(Redesignated TBP18S46)

SN54S475 (J) SN74S475 (J, N)  
(Redesignated TBP18SA46)

See Bipolar Microcomputer Components Data Book, second edition.

NC — No internal connection

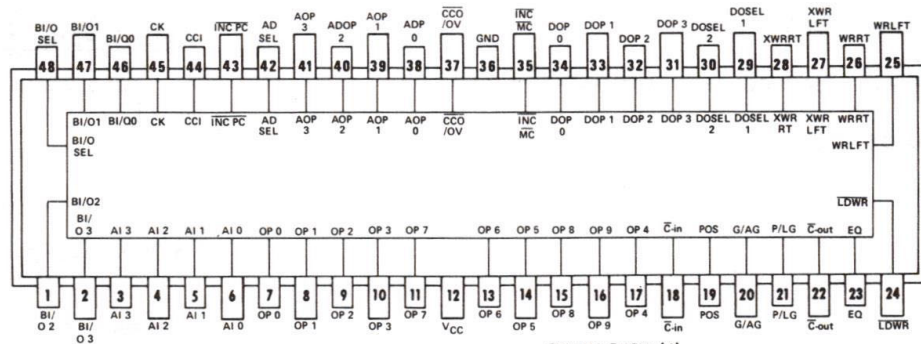


# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 4-BIT SLICE PROCESSOR ELEMENTS

**481**



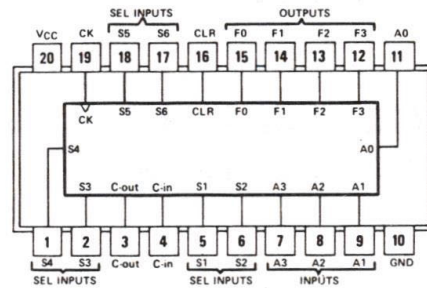
SN74LS481 (J)  
SN74S481 (J)

See Bipolar Microcomputer Components Data Book, second edition.

### 4-BIT-SLICE EXPANDABLE CONTROL ELEMENTS

**482**

CASCADABLE TO N-BITS

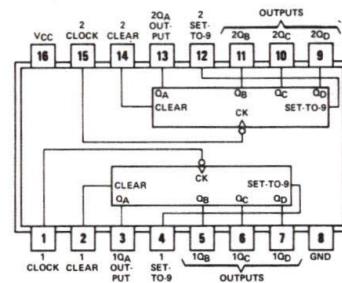


SN54S482 (J) SN74S482 (J, N)

See Bipolar Microcomputer Components Data Book, second edition.

### DUAL DECADE COUNTERS

**490**



SN54490 (J, W) SN74490 (J, N)  
SN54LS490 (J, W) SN74LS490 (J, N)

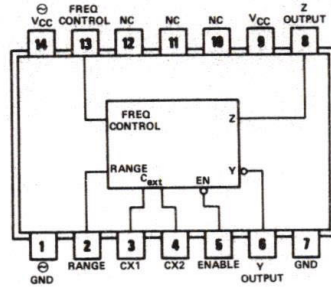
See page 7-520

# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### VOLTAGE-CONTROLLED OSCILLATORS

**624** TWO-PHASE OUTPUTS  
ENABLE CONTROL  
RANGE CONTROL

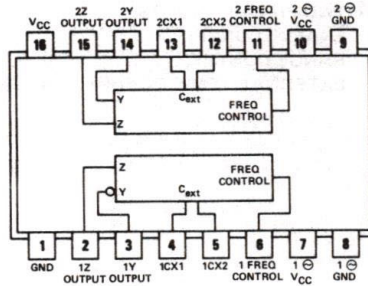


See page 7-460

SN54LS624 (J, W) SN74LS624 (J, N)

### DUAL VOLTAGE-CONTROLLED OSCILLATORS

**625** TWO-PHASE OUTPUTS

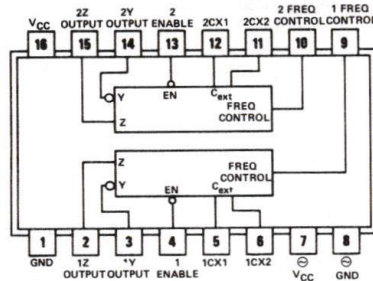


See page 7-460

SN54LS625 (J, W) SN74LS625 (J, N)

### DUAL VOLTAGE-CONTROLLED OSCILLATORS

**626** TWO-PHASE OUTPUTS  
ENABLE CONTROL



See page 7-460

SN54LS626 (J, W) SN74LS626 (J, N)

5

TEXAS INSTRUMENTS  
INCORPORATED

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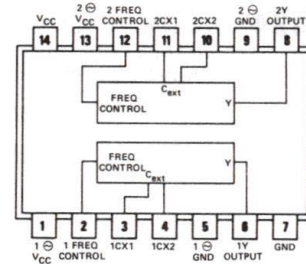
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# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### DUAL VOLTAGE-CONTROLLED OSCILLATORS

**627**

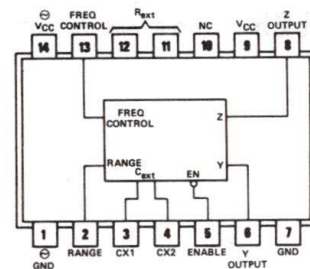


SN54LS627 (J, W) SN74LS627 (J, N)

See page 7-460

### VOLTAGE-CONTROLLED OSCILLATORS

**628** TWO-PHASE OUTPUTS  
ENABLE CONTROL  
RANGE CONTROL  
EXTERNAL TEMPERATURE COMPENSATION

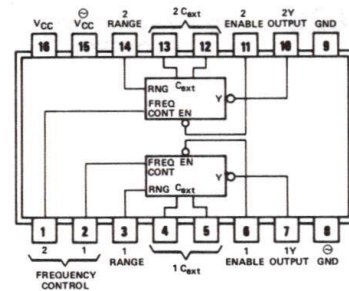


SN54LS628 (J, W) SN74LS628 (J, N)

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### DUAL VOLTAGE-CONTROLLED OSCILLATORS

**629** ENABLE CONTROL  
RANGE CONTROL



SN54LS629 (J, W) SN74LS629 (J, N)

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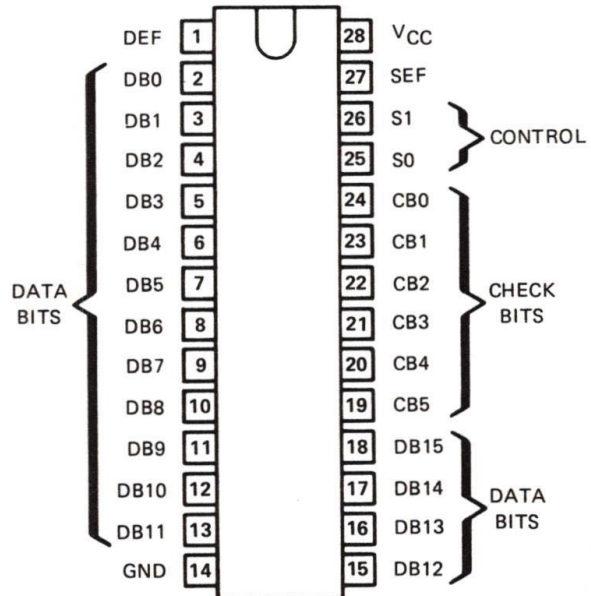
# 54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

## PIN ASSIGNMENTS (TOP VIEWS)

### 16-BIT ERROR DETECTION/CORRECTION CIRCUITS

**630** 3-STATE OUTPUTS

**631** OPEN-COLLECTOR OUTPUTS

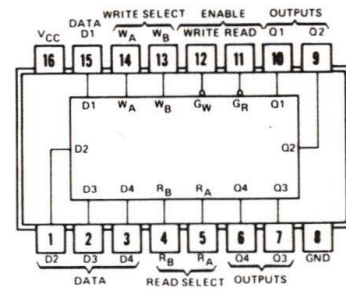


SN54LS630 (J) SN74LS630 (N)  
SN54LS631 (J) SN74LS631 (N)

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### 4-BY-4 REGISTER FILES

**670** 3-STATE OUTPUTS  
SIMULTANEOUS READ/WRITE  
EXPANDABLE TO 1024 WORDS



SN54LS670 (J, W) SN74LS670 (J, N)

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